M.Tech (EI), Two Year (Four Semesters)

Scheme to be valid with effect from the admitted batch of 2019 – 2020

MODEL QUESTION PAPERS

DIGITAL SIGNAL PROCESSING

Subject Code: MTEI-1.1 **Max Marks : 70**

Note : Answer any FIVE questions

1. A digital low-pass filter is required to meet the following specifications.
   (i) Pass band ripple ≤ 1 dB (ii) Pass band edge : 4 KHz (iii) Stop band attenuation ≥ 40 dB (iv) Stop band edge : 6 GHz (v) Sampling rate : 24 KHz
   The filter is to be designed by performing a bilinear transformation on an analog system function satisfying above specifications. Determine the order of butterworth, chebyshev and elliptic analog designs to be used to meet the specifications in the digital implementation. Determine the transfer function of the digital filter in each case.
   [14M]
2. (a) Explain about optimization methods for designing IIR filters and delay equalized elliptic filters.
   [7M]
   (b) Compare optimum FIR filters and delay equalized elliptic filters. [7M]
3. (a) Define (i) decimation (ii) interpolation and explain the process of decimation by factor 'D' [7M]
   (b) Decimating x(n) by a factor of D = 2 produces the signal $x_d(n) = x(2n)$ for all n shows that $x_d(n)$ and its transform $x_d(w)$. Do we lose any information when we decimate the sampled signal $x_s(n)$?
   [7M]
4. (a) Show that the linear interpolation is a second order approximation.
   [7M]
   (b) Explain the implementation of digital filter banks. [7M]
5. (a) Consider the ARMA process generated by the difference equation
   x(n) = 1.6x(n-1) - 0.6x (n-2) + w(n) + 0.9w(n-1)
   [7M]
   (i) Determine the system function of the whitening filter and its poles and zeros (ii) Determine the power density spectrum of {x(n)} [7M]
   (b) Illustrate how the whitening property of a prediction area filter and the AR modeling of a discrete time stochastic process are complementary.
   [7M]
6. (a) What is the role of wiener filters for filtering and prediction of signals.
   [6M]
   (b) Consider a signal x(n) = s(n) + w(n) where s(n) is an AR (1) Process that satisfies the difference equation. S(n) = 0.8 s(n-1) + v(n) where {v(n)} is a white noise sequence with variance $\sigma^2_v = 0.49$ and {w(n)} is a white noise sequence with variance $\sigma^2_w = 1$. The process {v(n)} and {w(n)} are uncorrelated (i) Determine the autocorrelation sequence $\{r_{ss}(m)\}$ and $\{r_{xx}(m)\}$. (ii) Design a wiener filter of length M = 2 to estimate {s(n)}
   (iii) Determine the MMSE for r = 2 [8M]
7. (a) Determine the reflection coefficient k_3 in terms of the autocorrelations $\{\psi_{xx}(m)\}$ from the scheme algorithm and compare your result with the expression for k_3 obtained from the Levinson Duebin algorithm.
   (b) Explain the Goertzel algorithm. If this algorithm fails which algorithm do you suggest ?

8. Describe the following [14M]

(i) Convolves

(ii) Channel vocoder TDM to FEM translate

ELECTRONIC INSTRUMENTATION TECHNIQUES

Subject Code: MTEI-1.2 **Max. Marks : 70**

Answer any Five Questions
All Questions Carry Equal Marks

1. (a) Explain the operation of a frequency synthesizer with the help of a functional block diagram.
   (b) Explain the principle of digital voltmeter with the help of a block schematic diagram. Explain the difference between a 4-digital and 3 ½ digit DVM.
2. (a) Draw the block diagram of a Q-meter and explain its operation. Show different arrangements in the circuit for (i) small impedances and (ii) large impedances.
   (b) A coil was tested using Q-meter and the following readings were obtained. At a frequency of 3 MHz, the value of capacitance to give a maximum voltage across the variable capacitor was 251 pF while at 6 MHz frequency it was 50 pF. Calculate the self-capacitance of the coil.
3. (a) With the help of a block diagram, explain the operation of a function generator. In what way does it differ from a signal generator?
   (b) Explain the need for frequency synthesizer. Explain with the help of a functional block diagram any type of frequency synthesizer.
4. (a) How do you differentiate between a spectrum analyzer, wave analyzer and a distortion analyzer.
   (b) Give the block diagram of a logic state analyzer and explain its operation. State its applications.
5. (a) With the help of a neat circuit diagram, explain the operation of a time base generator. Describe the various weep modes.
   (b) Write briefly about interference, shielding and grounding.
6. (a) Explain the principle of operation of magnetic tape recorder with special emphasis an recording head, reproducing head and tape transport mechanism.
   (b) Explain the principle of UV recorder.
7. (a) What are LEDs and LCDs? Explain in detail.
   (b) Write briefly about various displays.
8. Write short notes on the following.
   (a) Sampling oscilloscope
   (b) Lock-in-amplifier
   (c) Computer based automated test instruments.

MICROPROCESSOR SYSTEMS

Subject Code: MTEI-1.3(Elective-I) **Max. Marks : 70**

1. Draw the architectural block diagram of Intel 8051 microcontroller and explain the function of each block. [14]

2. (a) Draw the programming model of Intel 8086 and explain the function of registers and flags. [10]

   (b) Which instruction places the E-flags on the stock in the Pentium-IV microprocessor. [4]

3. (a) Explain the programming addressing modes and two stack memory addressing modes. [10]

   (b) Explain how LOOPE instruction operates [4]

4. (a) Explain how do you interface a 8259 A programmable intercept controller to 8086 microprocessor. [10]

   (b) Describe the differences between a protected mode and real mode intercept [4]

5. Describe how a direct memory access controller device an be connected to a 80686 system and describe how a DMA data transfer takes place [14]

6. (a) Explain with a block diagram how a co-processor can be connected to an 8086 operating in a maximum mode [10]

   (b) What ways are a standard microprocessor and a co-processor different from each other. [4]

7. Draw a 8-bit LED display interfaced to the 8086 microprocessor through an 82C55 PIA and explain the operation with the help of programming modes[14].

8. Write notes on any two of the following

   (a) RISC processor [7]
   (b) 8251 [7]
   (c) Interrupts used in 8086 [7]
   (d) differences between 8086 and 8088 [7]

Elective-II: EMI / EMC

Subject Code: MTEI – 1.4 **Max. Marks:** 70

Note: Answer any FIVE questions.

1 (a). List out the mechanisms in which EMI propagates from source to receiver and briefly explain the Electromagnetic spectrum and it's utilization. [7]

(b). List out sources of EMI in detail. [7]

2 (a). What is meant by ESD. Explain effects of lightening discharge on transmission lines. [7]

(b). Draw an ESD equivalent circuit and explain Electromagnetic pulse and it's impact. [7]

3 (a). Draw an equivalent circuit of relay / switching circuit and explain the characteristics of Electromagnetic noise produced by switches. [7]

(b). How do you explain phenomenon of crosstalk in transmission lines and list out materials to be used and materials to be avoided for reducing passive intermodulation.[7]

4 (a). Compare radiated interference test facilities in detail. [7]

(b) Explain the precautions to be taken in open area test site measurements. [7]

5 (a). Explain the conducted EM noise on power supply lines and conducted EMI from equipment and how do you eliminate them. [7]

(b). Describe different types of grounding techniques with suitable examples. [7]

6 (a). Define shielding effectiveness and explain different methods of shielding and design methodologies. [7]

(b). Describe characteristics of EMI filters. [7]

7 (a). Describe the characteristics of cables, connectors and compensators in EMC design. [7]

(b). Briefly discuss isolation transformers and optoisolators. [7]

8 . Write short notes on. [14]

(a) EMC Standards (b) Electrical bonding

(c) Electrical surges (d) Statistical EMI / EMC modules.

Elective-II: BIO-MEDICAL INSTRUMENTATION

Subject Code: MTEI-1.4 **Max. Marks: 70**

Note: Answer any Five Questions

1. (a) What are the resting and action potentials and explain in detail. (7)
   (b) Describe ECG and EEG waveforms. (7)
2. (a) What are the different types of Bio-electrodes and describe at least two of them. (7)
   (b) Describe bio-chemical transducer in detail. (7)
3. (a) Describe the function of the heart with a neat diagram. (7)
   (b) What is blood pressure and how do you measure it. (7)
4. (a) Draw ECG set-up and explain measurement mechanism. (7)
   (b) Describe plethysmography and measurement of heart sounds in detail. (7)
5. (a) Explain patient-monitoring displays in detail. (7)
   (b) Point out ICU equipment and describe them in briefly. (7)
6. (a) Describe two types of defibrillators. (7)
   (b) Draw the block diagram of bio-telemetry transmitter and receiver and explain. (7)
7. (a) Describe instrumentation for diagnostic x-rays. (7)
   (b) What are radiation therapy and explain in detail. (7)
8. Write short notes on (14)
   (a) Heart pacemakers
   (b) Bio-materials
   (c) Measurement of blood flow

TRANSDUCERS AND SIGNAL CONDITIONERS

Subject Code : MTEI-2.1 **Max Marks : 70**

Note : Answer any FIVE questions

1. (a) Define sensitivity of an instrument and explain zero drift and scale-factor drift in relation with sensitivity of an instrument. [7]

   (b) What are the factors influence the linearity of an electromechanical instrument and how it can be overcome. [7]

2. (a) How a mathematical model of a system differs from the physical model. With an example explain how a non-electrical system can be modeled. [7]

   (b) Obtain mathematical model of a first order RC high pass system subjected to the step excitation ? [7]

3. (a) Explain operation of magnetostrictive transducer for the measurement any one of the physical quantity. [7]

   (b) With digital methods how torque can be measured. [7]

4. (a) Explain the basic principle of measurement of sound suing different transducers ? [7]

   (b) Explain any of of the above method for measurement of sound in detail ? [7]

5. (a) What are the important parameters to be considered for the choice of selecting a transducer. [4]

   (b) Derive an expression for measurement of force using Piezo-electric transducer? [10]

6. (a) Explain any method to find the angular displacement with neat sketches? [7]

   (b) Explain how an angular displacement can be made with synchros and also derive an expression governing the angular displacement. [7]

7. (a) What are the advantages of Laser Doppler anemometer compared to ht wire anemometer? [3]

   (b) How to active the flow measurement using Doppler shift principle? [5]

   (c) In magnetic flow meter how flow level related with magnetic circuit elements? [6]

8. (a) What is the basic principle of measurement of vibrations and what are the quantities involved in the measurement of vibrations? [7]

   (b) With neat sketches explain the operation of seismograph? [7]

DATA ACQUISITION SYSTEM

Subject Code: MTEI-2.2 **Max. Marks: 70**

Answer any Five Questions
All Questions Carry Equal Marks

1. a) Draw the circuit diagram of a weighted resistor network D/A converter for a digital word 1100 and explain its operation.
   b) With the help of block schematic diagrams, suggest the data acquisition systems for the following and justify.
      ii) Signals of strength < 1 mVSignals of strength > 100 mV
2. a) Discuss the various DAS configurations presently in use. Compare the performance and limitations of each.
   b) Compare the performance of parallel DACs to serial DACs.
3. a) Explain the significance of different binary codes used in A to D and D to A converters.
   b) Write all the important specifications of D to A converter and explain DACs role in the construction of A to D converters?
4. a) What are the advantages of dual-slope ADC over single-slope ADC?
   b) The sampling rate of a sampled analog signal presented to the input of a successive approximation ADC is 5KHz. The flip-flops in the converter have a maximum guaranteed toggling rate of 2 MHz. What is the best possible resolution of the converter?
5. Bring out the different factors that see a limit on the accuracy of an ADC. Explain how static accuracy analysis is carried out for an ADC, with the help of error budget estimates. Illustrate your answer with an example.
6. a) Counter ramp A/D converters can be easily designed for high accuracy. Discuss/
   b) A 10-bit binary data is available in parallel form with binary '0' corresponding to 0V and binary 1 as 5 V. Design a suitable D/A converter. Assume any other data that may be required in the design. Draw the complete circuit diagram.
7. a) Give reasons for the following:
      i) The dual slope A/D converter can be designed so that it is unaffected by hum and noise related to power – supply frequency.
      ii) Digital display of measurement data is unsuitable if the data undergo small variations continuously.
   b) State the advantages of monolithic ADCs and DACs.
8. Write short notes on the following:
      a) Inverted ladder type DAC
      b) Logarithmic ADC
      c) Voltage to frequency conversion type ADC.

Elective III : GPS AND APPLICATIONS

Subject Code : MTEI-2.3 **Max. Marks:70**

Answer any Five Questions

1. (a) Describe the GPS Seattleite constellation with a neat diagram. (7)

   (b) How GPS aided Geo-augmented navigation (GAGAN) improves the GPS signal performance. (7)

2. Explain with a neat block diagram, the signal structure of L1 and L2 frequencies with the corresponding C/A, P- code and Navigation message (14)

3. (a) What are the important satellite orbital parameters that are used in the Satellite position computation in ECEF coordinate system (8)

   (b) What is WGS 84 system and how it is related to the GPS position computation (6)

4. (a) What is RINEX format (6)

   (b) Describe the Navigation message and Observation data files (8)

5. What are errors that are limiting the GPS system performance (7)

   (b) Describe ionospheric error with its contribution to the pseudorange estimation (7)

6. Explain with the relevant Equations, how the ionospheric error is eliminated in a two frequency GPS receiver (14)

7. (a) What is the difference between the Geo centric and Geodetic coordinate systems? (7)

   (b) Compare the GALILEO signal structure with the GPS signal structure (7)

8. Write any two of the following (14)

   (a) GPS time (b) Antispoofing (c) Selective Availability

Elective IV : MICROCONTROLLERS AND EMBEDDED SYSTEMS

Subject Code: MTEI-2.4 **Max. Marks:70**

Answer any Five Questions

1. (a) List and define the three main characteristics of embedded systems that distinguish such systems from other computing system. (2)
   (b) List and define the three IC technologies. What are the benefit of using each of the three different IC technologies. (4)
   (c) What is a Single-Purpose Processor? Design a custom Single-Purpose Processor? Explain with an example. (8)
2. (a) Explain the software development process of an embedded system. (7)
   (b) Enumerate the similarities and differences between a Microcontroller and Digital Signal Processor. (7)
3. (a) Given a 100MHz Crystal-Controlled Oscillator and a 32-bit and any number of 16-bit terminal counters. Design a relative clock that outputs the date and time down to milliseconds. You can ignore leap years. Draw a diagram and indicate terminal-count values for all counters. (9)
   (b) A watchdog timer uses two cascaded 16-bit up-counters is connected to an 11.981MHz oscillator . A time out should occur if the function watchdog-reset is not called within 5 minutes. What value should be loaded into the up-counter pair when the function is called. (5)
4. (a) Explain the cache impact on system performance with an example. (7)
   (b) Given the following three cache designs, find the one with best performance by calculating the average cost of access. Show all calculations.
      i. 4 Kbyte, 8-way set-associative cache with a 6% miss rate cache hit costs one cycle, cache miss cost 12 cycles.
      ii. 8 Kbyte, 4-way set-associative cache with a 4% miss rate cache hit costs two cycle, cache miss cost 12 cycles.
      iii. 16 Kbyte, 2-way set-associative cache with a 2% miss rate cache hit costs three cycle, cache miss cost 12 cycles. (7)
5. (a) Draw the timing diagram for a bus protocol that is handshaked non-addressed and transfers 8-bits of data over a 4-bit data bus. (7)
   (b) Explain the benefits an interrupt address table over fixed and vector interrupt methods. (7)
6. List the modifications made in Implementation: 2 (Microcontroller and CCDPP) and Implementation: 3 Microcontroller and CCDPP/ Fixed –Point DCT and discuss why each was beneficial in terms of performance. (14)

7. (a) Define the following terms: (7)

(i) Finite-state machines concurrent processor,

(ii) Real-time systems, and

(iii) Real-time operating systems.

(b) List three requirements of real-time systems and briefly describe each. Give examples of actual Real-time systems to support your arguments. (7)

8. Write notes on the following.

(a) Common Memory Types. (7)

(b) Stepper Motor Controllers. (7)

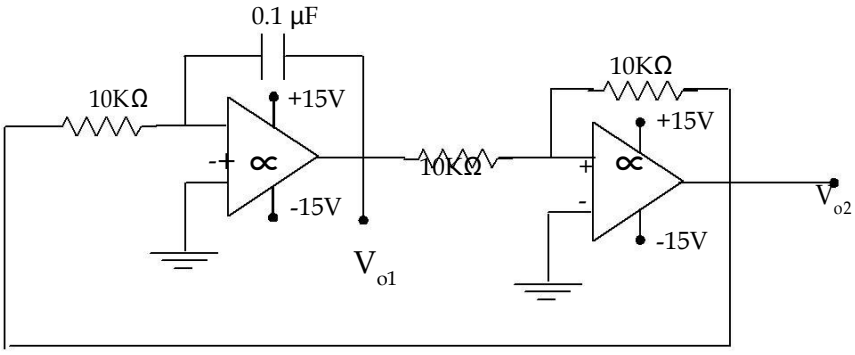
Elective-V: LINEAR AND DIGITAL SYSTEMS DESIGN

Subject Code: MTEI-3.1 **Max. Marks : 70**

Answer any Five Questions
All Questions Carry Equal Marks

1. (a) Distinguish between balancing and compensating of an operational amplifier. Explain the universal balancing circuit with neat circuit diagram. Explain also dominant pole frequency compensating technique with neat circuit diagram and frequency response characteristics?

   (b) For the circuit shown in figure, sketch the waveforms seen at V_{01} and V_{02} . Assume output saturation voltages of operational amplifiers are ± 15V.



2. (a) Design a Schmitt trigger circuit using an operational amplifier to set UTP = 4V and LTP = -2V. Use supply voltages of ± 15V. Explain its operation with the help of its transfer characteristics.

   (b) Design an astable multivibrator using 555 timer to get an output wave at 10 kHz square waveform with 30% duty cycle. Show the circuit diagram with all component values and explain its operation with waveforms. Discuss the limitations on the choice of passive components in your design.

3. (a) Explain the principle of operation of phase locked loop (PLL). Design PLL circuit using 565 IC to get (i) free running frequency = 4.5 kHz, (ii) lock range = 2 kHz, (iii) capture range = 100 Hz, (iv) power supply voltages = ± 10V. Explain its operation justifying your design.

   (b) Design a voltage regulator circuit using μA 723 IC to get an output voltage of 10V and load current of 1.0Amp. Give the specifications of the series pass transistor used.

4. (a) Draw the circuit diagram of a precision rectifier using operational amplifier and explain its operation with waveforms. Determine its sensitivity. Compare its band width with that of a passive rectifier.

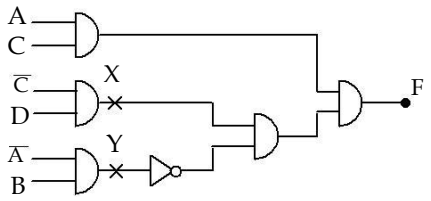
   (b) Draw the schematic diagram of a transconductance type four quadrant analog multiplier and explain its operation. Explain with neat block schematic diagrams its application as (i) squaring and square rooting, (ii) balanced modulator and (iii) phase sensitive detector.

5. (a) What is a priority encoder? Realize a 4 to 2 line priority encoder using minimum number of NAND gates.

   (b) Giving the necessary Boolean expressions, develop the block schematic diagram of a 4-bit carry look-ahead adder.

(c) Show the functional block diagram of a BCD adder and explain its operation with examples.

6. (a) Design a synchronous counter using JK flip-flop with the following binary sequence
   101 – 110 – 111 – 011 – 001 – 100 – 010 – 101
   (b) Obtain the complete structure of ROM for BCD to seven-segment display decoder application. The outputs of the ROM should control the display device.
7. (a) Design and realize a PLA circuit with four inputs X_1 , X_2 , X_3 and X_4 and seven outputs p_1 , p_2 , m_1 , m_2 , m_3 , m_4 and m_5 that receives BCD code words and generates the corresponding Hamming code words.
   (b) Design a six state R-Y-B phase sequence detector using ASM charts. Inputs are R, Y and B. If the sequence is R-Y-B output $Z_1 = 1$ and $Z_2 = 0$ and if the sequence is R-B-Y then the output $Z_1 = 0$ and $Z_2 = 1$. Assume suitable data.
8. (a) Construct a fault detection experiment to detect the following faults in the circuit shown below. (i) S-a-0 at X, (ii) S-a-1 at X, (iii) S-a-0 at Y and (iv) S-a-1 at Y.



   (b) Using "Quadded logic" desing a single fault tolerant circuit to realize the function $F(AB) = A'B' + AB$.

Elective-V : OPTICAL FIBERS AND APPLICATIONS

Subject Code: MTEI-3.1 **Max Marks : 70**

Note : Answer any FIVE questions

1. a) Discuss the properties and characteristics of Optical fibers 7
   b) Explain the difference between a step-index fiber and a graded index fiber. 7 What are the advantages of using graded index core in a fiber?

2. a) Explain the principle of operation of LED. Enumerate the characteristics of LED 7
   b) Discuss the operation of an Avalanche Photodiode. Explain the factors that limit the time response of Avalanche photodiode. 7

3. a) Explain the operation of a LASER. 6
   b) Explain the following properties of LASER : 8
   i) Line Width ii) Beam Divergence angle

4. a) With neat diagrams explain the various types of splicing and source couplings used in optical fibers. 7
   b) Explain the principle of operation of i) Optical fiber isolator ii) Optical attenuator 7

5. a) What is system risk time?. Explain how does it limit an optical fiber communication link. 7
   b) Explain quantum limit.A certain optical fiber link at 850 nm requires maximum bit error rate(BER) = 10^{-9} . Find the quantum current at a data rate of 10 Mb/Sec. (Assume h= 6.626 X 10^{-34} J-Sec) 7

6 a) Draw the block diagram of an optical receiver and give the noise equivalent circuit of the voltage amplifier. 6
   b) Explain the principle of operations of Photo detectors and photo multipliers. 8

7 a) What is multiplexing?. Explain in detail the Wavelength division multiplexing. 7
   b) Explain various network topologies in multiplexing fiber optic sensors. 7

8 Write short notes on: 14
   a) PIN photo diodes
   b) Fiber Bragg Gratings
   c) Digital System design.

VLSI

Subject Code : MTEI-3.2 Max Marks : 70

Note : Answer any FIVE questions

1. a. Explain different processes involved in the fabrication of CMOS transistor with necessary cross sectional diagrams. (7)
   b. Discuss the body effect and latch up phenomena related to CMOS structures and suggest remedies for these problems. (7)
2. a. Determine the pull up and pull down ration for an NMOS inverting logic coupled by pass transistors. (7)
   b. Explain the sheet resistance, standard unit of capacitance and delay related to NMOS and CMOS technologies. (7)
3. a. Explain about inverter delays and estimate the rise time, fall time of a CMOS inverter delay. (7)
   b. Discuss the following forms of CMOS logic. (7)

      i. Pseudo NMOS logic
      ii. Dynamic CMOS logic and
      III. C^2 MOS logic
4. a. Give the organization of layout of typical standard cell. (7)
   b. Explain in detail the limits on logic levels and supply voltage due to noise in the scaling of devices. (7)
5. a. Explain how a flip flop is realized using NMOS and CMOS. (7)
   b. Explain the design of a 4 bit shift register. (7)
6. a. Explain the need for testing in CMOS chip fabrication. Compare chip level testing and system level testing. Give different test design strategies. (8)

   b. Give the cross section of one transistor DRAM cell built with trench capacitor and explain its working. (6)
7. a. Give a neat schematic of typical PAL structure and explain the different ways of programming. (7)
   b. What are VLSI CAD tools ? Explain design capture tools. (7)

8. Write short notes on the following.
   a. Stick diagrams. (4)
   b. Testing of combinational circuits. (6)
   c. Sub system design tools. (4)