ANDHRA UNIVERSITY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



PROGRAM : M.TECH(VLSI) REGULATION AND SYLLABUS EFFECTIVE FROM 2019-2020 BATCH

Dept. of Electronics & Communications Engineering Andhra University College of Engineering (A) Visakhapatnam-530003



M.TECH VLSI

 $Scheme of Instruction and Examination \ with effect \ from \ 2019-2020 \ admitted \ batchonwards$

Under AICTE Model Curriculum

M.Tech (VLSI), B.Tech+M.Tech(5/6 and 6/6), Two Year (Four Semesters)

Scheme to be valid with effect from the admitted batch of 2019 - 2020

Code	Name of the Subject	Periods/Week		Max.		Total	Credits
				Ma	rks		
		Theory	Lab	Ext.	Int.		
MTVL1.1	VLSI Design Techniques	3	-	70	30	100	3
MTVL1.2	Analog IC design	3	-	70	30	100	3
MTVL1.3	Elective – I (Digital Signal Processing/ Application Specific Integrated Circuit(ASIC)/ Hardware Software Co Design/ Advanced Microprocessors & Microcontrollers)	3	_	70	30	100	3
MTVL1.4	Elective – II (CPLD and FPGA Architecture & Applications / VHDL Modelling of Digital Systems/EDA Tools)	3	-	70	30	100	3
MTVL1.5	Research Methodology & IPR	3	-	70	30	100	2
MTVL1.6	Audit Course	3	-	-	100	100	0
MTVL1.7	HDL Programming LAB-I	-	3	-	100	100	2
MTVL1.8	Analog IC Design LAB	-	3	-	100	100	2
		18	6	350	450	800	18

I-Semester

II-Semester

Code	Name of the Subject	Periods/Week		Max.		Total	Credits
				Marks			
		Theory	Lab	Ext.	Int.		
MTVL2.1	Digital System Design	3	-	70	30	100	3
MTVL2.2	Algorithms for VLSI design automation	3	-	70	30	100	3
MTVL2.3	Elective – III (Low Power VLSI Design/ Wireless Communication and networks/ RF& Microwave Integrate Circuits)	3	-	70	30	100	3
MTVL2.4	Elective – IV (Microcontroller and Embedded Systems/ Digital	3	-	70	30	100	3

	Systems Testing & Testable Design/ DSP Processors and Architectures)						
MTVL2.5	Audit Course	3	-	-	100	100	0
MTVL2.6	HDL Programming LAB-II	-	3	-	100	100	2
MTVL2.7	Mixed Signal Simulation LAB	-	3	-	100	100	2
MTVL2.8	Mini Project with Seminar	-	3	-	100	100	2
		15	9	280	520	800	18

Code	Name of the Subject	Periods/W	/eek	Ma	ıx.	Total	Credits
				Marks			
		Theory	Lab	Ext.	Int.		
MTVL3.1	Elective – V System Modeling and Simulation/ EMI/EMC/Hardware Software Co Design	3	_	70	30	100	3
MTVL3.2	Open Elective Cellular & Mobile Communications Business Analytics Industrial Safety Operational Research Cost Management of Engineering Projects	3	_	70	30	100	3
MTVL3.3	Dissertation- I / Industrial Project	-	-	100		100	10
		6	-	240	60	300	16

III-Semester

IV-Semester

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL4.1	Dissertation-II	-	-	100	-	100	16
		-	-	100	-	100	16

Audit Course 1 & 2

- 1. English for Research Paper Writing
- 2. Disaster Management
- 3. Sanskrit for Technical Knowledge
- 4. Value Education
- 5. Constitution of India
- 6. Pedagogy Studies
- 7. Stress Management by Yoga
- 8. Personality Development through Life Enlightenment Skills

Andhra University College of Engineering Andhra University

Department of Electronics and Communication Engineering

PROGRAMME: B.Tech (Electronics and Communication Engineering)

Programme Specific Outcomes (PSOs)

The Graduate of ECE will be able to:

Communication Engineering to identify, investigate and solve various real-life problems in the field of Electronics.
Graduates will be able to design and develop systems in the emerging electronics and communication allied disciplines to meet out the industry challenges.
Graduates will be able to demonstrate the leadership qualities and strive for the betterment of organization, environment and society with professional and ethical responsibilities

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The Graduates of ECE will be able to:

- 1. To provide an in-depth knowledge in the fundamental and advanced areas of electronics and communication engineering and there by excel in professional career and/or higher education.
- 2. To train students in the software/hardware design of electronics and communication systems and can promote the development of research activity as well as innovation and entrepreneurship that caters to theneed of Industry and Society.
- 3. To develop technical skill set for solving real life problems.
- 4. To develop qualities like creativity, leadership, team work, and professional ethics for contributing towards the growth and development of society.
- 5. To inculcate in students professional and ethical attitude, and an ability to relate engineering issues to broader social context.

	Program Outcomes		EC	E Graduates	will	be able to	
PO1	Engineering knowledge	Apply engineer commun	the ing fu ication	knowledge ndamentals to n problems	of real	mathematics, time electronics	science, and

PO2	Problem analysis	Provide solutions for ECE problems by Identify, formulate, review literature, analyze, designing and conducting experiments, interpreting and reporting the results.
PO3	Design/development of solutions	Design and develop solutions for complex engineering problems at feasible and optimal solutions that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage	Select and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society	Apply contextual knowledge to assess industrial, societal and safety related issues and understand consequent relevance to the professional engineering practice.
PO7	Environment and sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication	Communicate effectively on complex engineering activities with the engineering community and with societyat large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	Project management and finance	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long learning	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME: B.Tech + M.Tech (Electronics and Communication Engineering)

Programme Specific Outcomes (PSOs)

The Graduate of ECE will be able to:

PSO-1	Graduates will be able to apply fundamental knowledge of Electronics and Communication Engineering to identify, investigate and solve various real-life problems in the field of Electronics.
PSO-2	Graduates will be able to design and develop systems in the emerging electronics and communication allied disciplines to meet out the industry challenges.
PSO-3	Graduates will be able to demonstrate the leadership qualities and strive for the betterment of organization, environment and society with professional and ethical responsibilities.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The Graduates of ECE will be able to:

- 1. To provide an in-depth knowledge in the fundamental and advanced areas of electronics and communication engineering and there by excel in professional career and/or higher education.
- 2. To train students in the software/hardware design of electronics and communication systems and can promote the development of research activity as wellas innovation and entrepreneurship that caters to theneed of Industry and Society.
- 3. To develop technical skill set for solving real life problems.
- 4. To develop qualities like creativity, leadership, team work, and professional ethics forcontributing towards the growth and development of society.
- 5. To inculcate in students professional and ethical attitude, and an ability to relate engineering issues to broader social context.

	Program Outcomes	ECE Graduates will be able to
PO1	Engineering knowledge	Apply the knowledge of mathematics, science, engineering fundamentals to real time electronics and communication problems.
PO2	Problem analysis	Provide solutions for ECE problems by Identify, formulate, review literature, analyze, designing and conducting experiments, interpreting and reporting the results.

PO3	Design/development of solutions	Design and develop solutions for complex engineering problems at feasible and optimal solutions that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage	Select and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society	Apply contextual knowledge to assess industrial, societal and safety related issues and understand consequent relevance to the professional engineering practice.
PO7	Environment and sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication	Communicate effectively on complex engineering activities with the engineering community and with societyat large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	Project management and finance	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long learning	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME: M.Tech (Electronic Instrumentation)

Programme Specific Outcomes (PSOs)

The Post Graduate of EI will be able to:

PSO-1	Analyze specific problems relevant to Electronic Instrumentation by applying the knowledge of basic sciences, Instrumentation fundamentals and advancements to solve technical problems.
PSO-2	Electronic Instrumentation Engineers, including supportive and leadership roles in multidisciplinary domain and Design of electronic devices, software and hardware using the significant analytical knowledge in instrumentation by applying modern tools.
PSO-3	Apply and transfer interdisciplinary systems and Engineering approaches to the various areas like communication etc.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The Post Graduates of EI will be able to:

- 1. Identify and apply appropriate experimental and analytical skills to solve real world problems in Electronic Instrumentation field to create innovative products and systems.
- 2. Develop technical skills and apply appropriate techniques to formulate and analyze engineering problems in Instrumentation and Process Control.
- 3. Pursue career in research in multidisciplinary areas of signal processing, image processing and instrumentation domain through self-learning and self-directed on futuristic cutting-edge technologies.
- 4. Analyze technical problems and develop feasible, optimal, environmentally and socially acceptable solutions by applying research skills, technological knowledge and modern tools while working individually and in teams.
- 5. Students will be able to function professionally in rapidly changing world due to advances in electronics and related technologies in order to contribute to the needs of the society.

	Program Outcomes	EI Post Graduates will be able to			
PO1	Engineering knowledge	Acquire in depth knowledge in the domain of Electronic Instrumentation Engineering.			

PO2	Problem analysis	Understand various Electronic and Instrumentation strategies and their applications for various types of systems.					
PO3	Design/development of solutions	Design solutions for complex Electronic Instrumentation problems and design components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal and environmental considerations.					
PO4	Conduct investigations of complex problems	Demonstrate implementation skills using advanced software and processing techniques.					
PO5	Modern tool usage	Use recent state-of-the-art simulation tools in the field of BioMedical engineering such as MATLAB, MULTISIM PYTHON, LABVIEW and other Tools.					
PO6	The engineer and society	Be capable of contribute positively to collaborative and multidisciplinary research to achieve common goals.					
PO7	Environment and sustainability	Demonstrate knowledge and understanding of Electronic Instrumentation engineering and management principles and Undertake research in emerging areas of Instrumentation with due consideration to economical, Environment and financial factors.					
PO8	Ethics	Become aware of social issues and become socially responsible and follow ethical practices to contribute to the community for sustainable development of society.					
PO9	Individual and team work	Capable of analyzing the work independently and reflective learning while developing project in the team with multidisciplinary settings.					
		Communicate confidently, make effective presentations					
PO10	Communication	and write good reports to engineering community and society.					
PO11	Project management and finance	Independently observe and examine critically the outcomes of his/her actions, apply corrective measures subsequently and move forward positively through a self-corrective approach.					
PO12	Life-long learning	Recognize the need for life-long learning and have the ability to do it independently in the domain of Electronic Instrumentation engineering.					

PROGRAMME: M.Tech (Radar and Microwave)

Programme Specific Outcomes (PSOs)

The Post Graduate of R&M will be able to:

PSO-1	To analyze, design and develop solutions for the real time problems and to apply the technical knowledge for developing quality products for Radar and Microwave industry.	
PSO-2	To adapt to emerging information and communication technologies and to develop innovative ideas and solutions in Radar and Microwave.	
PSO-3	To design Radar and Microwave containing devices, software, and hardware by applying relevant modern tools.	

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The Post Graduates of R&M will be able to:

- 1. Work in educational, R&D institutes, industry, and as an entrepreneur in Radar & Microwave.
- 2. Pursue their doctoral studies and research in institutes of high repute in India & abroad and develop independent and lifelong learning skills for continuous professional development.
- 3. Analyze technical problems and develop feasible, optimal, environmentally, and socially acceptable solutions by applying research skills, technical knowledge, and modern tools while working individually and in teams.
- 4. To inculcate the culture of research-oriented projects in the Radar and Microwave field.
- 5. Demonstrate an ability to communicate effectively and practice professional ethics and Social responsibility in their career.

Program Outcomes		R&M Post Graduates will be able to				
PO1	Engineering knowledge	Acquire in-depth knowledge of RF and Microwave communication with an ability to evaluate, analyze and Synthesize complex problems.				
PO2	Problem analysis	Conceptualize and solve engineering problems, to arrive at optimal solutions, considering public health and safety, societal and environmental factors.				
PO3	Design/development of solutions	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.				
PO4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.				
PO5	Modern tool usage	Create, select and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.				
PO6	The engineer and society	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.				
PO7	Environment and sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.				
PO8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.				
PO9	Individual and team work	Function effectively as an individual, and as a number or leader in diverse teams and in multidisciplinary settings.				

PO10	Communication	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations and give and receive clear instructions.
PO11	Project management and finance	Demonstrate knowledge and understanding of the engineering and management principles and apply there to one's own work, add a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long learning	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME: M.Tech (VLSI)

Programme Specific Outcomes (PSOs)

The Post Graduate of VLSI will be able to:

PSO-1	An ability to understand the concepts of VLSI and to master the latest tools and techniques used in the field of research and industry.
PSO-2	To adapt to emerging information and communication technologies and to develop innovative ideas and solutions in VLSI.
PSO-3	An understanding of social awareness & environmental wisdom along with ethical responsibility to achieve a successful career and to sustain passion and zeal for real world applications.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The Post Graduates of VLSI will be able to:

- 1. Identify and apply appropriate experimental and analytical skills to solve real world problems in VLSI to create innovative products and systems.
- 2. Pursue their doctoral studies and research in institutes of high repute in India & abroad and develop independent and lifelong learning skills for continuous professional development.
- 3. Students will be able to function professionally in rapidly changing world due to the advances in VLSI and related technologies in order to contribute to the needs of the society.
- 4. Develop an ability to analyze the problem, understand the technical requirements, design and deliver engineering solutions and create effective product design.
- 5. To inculcate the culture of research-oriented projects in VLSI.

	Program Outcomes	VLSI Post Graduates will be able to					
PO1	Engineering knowledge	Apply the knowledge of mathematics, science, engineering fundamentals to real time electronics and communication problems.					

PO2	Problem analysis	Provide solutions for ECE problems by Identify, formulate, review literature, analyze, designing and conducting experiments, interpreting and reporting the results.
PO3	Design/development of solutions	Design and develop solutions for complex engineering problems at feasible and optimal solutions that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	Modern tool usage	Select and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society	Apply contextual knowledge to assess industrial, societal and safety related issues and understand consequent relevance to the professional engineering practice.
PO7	Environment and sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual and team work	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication	Communicate effectively on complex engineering activities with the engineering community and with societyat large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	Project management and finance	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	Life-long learning	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAMME: M.Tech (BioMedical Engineering)

Programme Specific Outcomes (PSOs)

The Post Graduate of BME will be able to:

PSO-1	Analyze specific problems relevant to BioMedical Engineering by applying the knowledge of basic sciences, BioMedical Instrumentation fundamentals and advancements to solve technical problems.
PSO-2	To adapt emerging technologies and to develop innovative ideas and solutions in Biomedical Engineering.
PSO-3	An ability to make use of acquired technical knowledge to get employed in the field of BioMedical.

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The Post Graduates of BME will be able to:

- 1. Identify and apply appropriate experimental and analytical skills to solve real world problems in the field of BioMedical Engineering to create innovative products and systems.
- 2. Develop technical skills and apply appropriate techniques to formulate and analyze engineering problems in BioMedical Instrumentation.
- 3. Pursue career in research in multidisciplinary areas of Biomedical signal processing, Biomedical image processing and instrumentation domain.
- 4. Analyze technical problems and develop feasible, optimal, environmentally and socially acceptable solutions by applying research skills, technological knowledge and modern tools while working individually and in teams.
- 5. Students will be able to function professionally in rapidly changing world due to advances in Biomedical and related technologies in order to contribute to the needs of the society.

	Program Outcomes	BME Post Graduates will be able to					
PO1	Engineering knowledge	Acquire in depth knowledge in the domain of BioMedical Engineering.					
PO2	Problem analysis	Understand various BioMedical strategies and their applications for various types of systems.					

PO3	Design/development of solutions	Design solutions for complex Biomedical problems and design components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal and environmental considerations.			
PO4	Conduct investigations of complex problems	Demonstrate implementation skills using advanced software and processing techniques.			
PO5	Modern tool usage	Use recent state-of-the-art simulation tools in the field of BioMedical engineering such as MATLAB, PYTHON, LABVIEW and other Tools.			
PO6	The engineer and society	Be capable of contribute positively to collaborative and multidisciplinary research to achieve common goals.			
PO7	Environment and sustainability	Demonstrate knowledge and understanding of BioMedical engineering and management principles and Undertake research in emerging areas of BioMedical with due consideration to economical, Environment and financial factors.			
PO8	Ethics	Become aware of social issues and become socially responsible and follow ethical practices to contribute to the community for sustainable development of society.			
PO9	Individual and team work	Capable of analyzing the work independently and reflective learning while developing project in the team with multidisciplinary settings.			
PO10	Communication	Communicate confidently, make effective presentations and write good reports to engineering community and society.			
PO11	Project management and finance	Independently observe and examine critically the outcomes of his/her actions, apply corrective measures subsequently and move forward positively through a self-corrective approach.			
PO12	Life-long learning	Recognize the need for life-long learning and have the ability to do it independently in the domain of BioMedical engineering.			

Dept. of Electronics & Communications Engineering Andhra University College of Engineering (A) Visakhapatnam-530003



M.TECH VLSI

 $Scheme of Instruction and Examination \ with effect \ from \ 2019-2020 \ admitted \ batchonwards$

Under AICTE Model Curriculum

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Scheme to be valid with effect from the admitted batch of 2019 - 2020

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	_			Marks			
		Theory	Lab	Ext.	Int.		
MTVL1.1	VLSI Design Techniques	3	-	70	30	100	3
MTVL1.2	Analog IC design	3	-	70	30	100	3
MTVL1.3	Elective – I (Digital Signal Processing/ Application Specific Integrated Circuit(ASIC)/ Hardware Software Co Design/ Advanced Microprocessors & Microcontrollers)	3	_	70	30	100	3
MTVL1.4	Elective – II (CPLD and FPGA Architecture & Applications / VHDL Modelling of Digital Systems/EDA Tools)	3	-	70	30	100	3
MTVL1.5	Research Methodology & IPR	3	-	70	30	100	2
MTVL1.6	Audit Course	3	-	-	100	100	0
MTVL1.7	HDL Programming LAB-I	-	3	-	100	100	2
MTVL1.8	Analog IC Design LAB	-	3	-	100	100	2
		18	6	350	450	800	18

I-Semester

II-Semester

Code	Name of the Subject	Periods/Week		Max.		Total	Credits
				Marks			
		Theory	Lab	Ext.	Int.		
MTVL2.1	Digital System Design	3	-	70	30	100	3
MTVL2.2	Algorithms for VLSI design automation	3	-	70	30	100	3
MTVL2.3	Elective – III (Low Power VLSI Design/ Wireless Communication and networks/ RF& Microwave Integrate Circuits)	3	-	70	30	100	3
MTVL2.4	Elective – IV (Microcontroller and Embedded Systems/ Digital	3	-	70	30	100	3

	Systems Testing & Testable Design/ DSP Processors and Architectures)						
MTVL2.5	Audit Course	3	-	-	100	100	0
MTVL2.6	HDL Programming LAB-II	-	3	-	100	100	2
MTVL2.7	Mixed Signal Simulation LAB	-	3	-	100	100	2
MTVL2.8	Mini Project with Seminar	-	3	-	100	100	2
		15	9	280	520	800	18

Code	Name of the Subject	Periods/Week		Ma	ıx.	Total	Credits	
				Marks				
		Theory	Lab	Ext.	Int.			
MTVL3.1	Elective – V System Modeling and Simulation/ EMI/EMC/Hardware Software Co Design	3	_	70	30	100	3	
MTVL3.2	Open Elective Cellular & Mobile Communications Business Analytics Industrial Safety Operational Research Cost Management of Engineering Projects	3	_	70	30	100	3	
MTVL3.3	Dissertation- I / Industrial Project	-	-	100		100	10	
		6	-	240	60	300	16	

III-Semester

IV-Semester

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL4.1	Dissertation-II	-	-	100	-	100	16
		-	-	100	-	100	16

Audit Course 1 & 2

- 1. English for Research Paper Writing
- 2. Disaster Management
- 3. Sanskrit for Technical Knowledge
- 4. Value Education
- 5. Constitution of India
- 6. Pedagogy Studies
- 7. Stress Management by Yoga
- 8. Personality Development through Life Enlightenment Skills

VLSI DESIGN TECHNIQUES

Credits : 3

Subject Code :MTVL – 1.1 I – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: Attain mastery in applying VLSI concepts to Engineering problems so as to meet the need of the industry, teaching, higher education or research.

CEO 2:To understand other process steps like etching, implantation and metallization and their implications.

CEO 3:To understand the semiconductor materials, devices and technology historical evaluations

CEO 4:To explain the oxidization process and quality measures in the fabrication

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Identify the various design limits material used for fabrication.

CO 2::Describe the Performance of technology scaling

CO 3::Understand the complexities involved in the integrated circuits

CO 4: Apply principles to Identify and Analyze the various steps for the fabrication of various components

CO 5: Assess the various reliability issues in VLSI technology

UNIT- I

INTRODUCTION: Basic Principle of MOS Transistor, Introduction to Large Signal MOS Models(Long Channel) For Digital Design.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:Explain basic principle of Mos transistor

LO 2:understand large signal MOS Models for digital design

UNIT –II

THE MOS INVERTER, LAYOUT AND SIMULATION:Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption. MOS SPICE Model, Device Characterization, Circuit Characterization, Interconnects and Simulation. MOS Device Layout, Transistor Layout, Inverter Layout, CMOS Digital Circuits Layout & Simulation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:Explain basic principle of inverter

LO 2:understand transfer characteristics of CMOS inverter

LO 3: observe simulation of CMOS digital circuits

UNIT-III

COMBINATIONAL MOS LOGIC DESIGN: Static MOS design; Complementary MOS,Rationed logic, Pass Transistor logic, complex logic circuits, Dynamic MOS Design, Dynamic Logic Families and Performances.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:design static MOS

LO 2:design complex logic circuits

LO 3:observe performances of dynamic logic families.

UNIT –IV

SEQUENTIAL MOS LOGIC DESIGN: Static Latches, Flip Flops and Registers, DynamicLatches and Registers, CMOS Schmitt trigger, Monostable Sequential Circuits, Astable Circuits, Memory Design, ROM and RAM Cells Design.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:design of latches and flipflops.

- LO 2:design of sequential circuits.
- LO 3:design of various memory cell designs.

UNIT –V

INTERCONNECT AND CLOCK DISTRIBUTION: Interconnect Delays, Cross Talks, ClockDistribution. Introduction to Low- power Design, Input and Output Interface circuits.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand interconnect delays and cross talks.

- LO 2:explain clock distribution.
- LO 3:understand low power design.

UNIT-VI

BICMOS LOGIC CIRCUITS: Introduction, BJT Structure and Operation, Basic BiCMOSCircuit behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain BJT structures

LO 2:understand basic BICMOS circuit

LO 3:explain applications of BICMOS.

TEXT BOOKS:

- 1. Kang &Leblebigi "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003
- 2. Rabey, "Digital Integrated Circuits Design", Pearson Education, Second Edition, 2003

REFERENCE:

1. Weste and Eshraghian, "Principles of CMOS VLSI design" Addison-Wesley, 2002

ANALOG IC DESIGN

Credits : 3

Subject Code: MTVL – 1.2 I – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To understand the construction, operation and mathematical models of MOSFETs.

CEO 2:To study and analyze different current mirrors used to bias IC amplifiers.

CEO 3:To understand the frequency response of amplifier designed in integrated circuits

CEO 4:To understand different specifications and topologies related to operational amplifiers.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:acquire knowledge of device physics related to MOSFET

CO 2:acquire knowledge of amplifier design with the use of proper biasing techniques

CO 3:identify appropriate circuit topology for given gain, input impedance, output impedance and bandwidth requirements

CO 4:design feedback circuits to meet the given gain error, bandwidth, input and output impedance requirements

CO 5:• acquire the knowledge of different op-amp topologies and to design opamps for the given specifications

UNIT-I

INTEGRATED CIRCUIT DEVICES AND MODELLING: MOS Transistors,

AdvancedMOS Modeling, Bipolar Junction Transistors, Device Model Summary, SPICE Modelling Parameters.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain MOS Transistor and BJT.

LO 2:understand the advanced MOS Modeling

LO 3: analyze the SPICE modeling parameters.

UNIT-II

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: Simple CMOS

CurrentMirror, Common Source, Source-Follower, Common Gate Amplifier, High-Output-Impedance Current Mirrors and Bipolar Gain Stages, Frequency Response. **Learning Outcomes:** At the end of the unit, the student will be able to

LO 1:explain CMOS current mirrors.

LO 2:understand CS,CG amplifiers

LO 3:observe frequency response of current mirrors.

UNIT –III

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOSOperational Amplifier, Feedback and Operational Amplifier Compensation, Comparator, Charge Injection Error, Latched Comparator and Bi CMOS Comparators.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:explain feedback and OPAMP compensation.
- **LO 2:**understand charge injection error.
- LO 3:understand BICMOS comparators

UNIT –IV

ADVANCED CURRENT MIRRORS AND OPERATIONAL AMPLIFIERS:

AdvancedCurrent Mirror, Folded–Cascade Operational Amplifier, Current-Mirror Operational Amplifier, Fully Differential Operational Amplifiers, Common-Mode Feedback Circuits, Current-Feedback Operational Amplifiers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:Understand advanced Current mirror

LO 2:understand current mirror OPAMP

LO 3: explain feedback circuits of OPAMP.

UNIT-V

SAMPLE AND HOLD, **SWITCHED-CAPACITOR CIRCUITS:** MOS Sample-and-Hold Basics, CMOS Sample and Hold Circuits, Bipolar and BiCMOS Sample and Holds.Basic Operation and Analysis, First-Order and Biquad Filters, Charge Injection, Switched-Capacitor Gain Circuits, Correlated Double-Sampling Techniques, Other Switched-Capacitor circuits.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand basics of mos sample and hold.

LO 2:analysis of biquad filters

LO 3:explain various gain circuits and techniques.

UNIT- VI

DATA CONVERTERS: Ideal D/A & A/D Converters, Quantization Noise, PerformanceLimitations, Nyquist-Rate D/A Converters: Decoder Based Converters, Binary-Scaled Converters, Hybrid Converters, Nyquist-Rate A/D Converters, Integrating, Successive-Approximation, Cyclic Flash Type, Two-Step A/D Converters, Interpolating A/D Converters, Folding A/D Converters and Pipelined A/D Converters. Over Sampling with and without Noise Shaping, Digital Decimation Filter, Higher-Order Modulators, Bandpass Oversampling Converter.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:explain A/D & D/A converter.
- LO 2:understand various types of converters.
- LO 3:explain sampling techniques.

TEXT BOOKS:

1. I.D.A.JOHN& KEN MARTIN; Analog Integrated circuit design. John Wiley, 1997

REFERENCE:

1. GREGOLIAN & TEMES: Analog MOS Integrated Circuits, John Wiley, 1986

Elective-I

DIGITAL SIGNAL PROCESSING

Credits : 3

Subject Code :MTVL – 1.3 I – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: designed to give students the required knowledge for DFT, FFT, Z Transforms and its computation and understand the design techniques for digital filters

CEO 2:Thorough understanding of frequency domain analysis of discrete time signals

CEO 3: Ability to design & analyze DSP systems like FIR and IIR Filter etc

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Analyze discrete-time signals and systems in various domains

CO 2:Design and implement filters using fixed point arithmetic targeted for embedded platforms

CO 3:Acquire the basics of multi rate digital signal processing.

CO 4:: Comprehend the DFTs and FFTs

CO 5:Comprehend the Finite word length effects in Fixed point DSP Systems.

UNIT-I

ADVANCED DIGITAL FILTER DESIGN TECHNIQUES:Multiple Band Optimal FIRFilters, Design of Filters with Simultaneous Constraints in Time and Frequency Response, Optimization Methods for Designing IR Filters, Comparison of Optimum FIR Filters and Delay Equalized Elliptic Filters.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:design FIR filters

LO 2:Design IIR filters

LO 3:understand the comparison of different types of filters

UNIT-II

MULTI-RATE DIGITAL SIGNAL PROCESSING: The basic sample rate alteration – Time – Domain Characterization, Frequency – Domain Characterization: Cascade Equivalences, Filters in Sampling Rate Alteration Systems.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:understand the time domain characterization.
- LO 2: understand the frequency domain characterization.
- LO 3:explain filters in sampling rate alteration

UNIT-III

DIGITAL FILTER BANKS AND OPTIMUM LINEAR FILTERS: Analysis of DigitalFilter Banks and their Applications, Multi Level Filter Banks, Estimations of Spectra from Finite – Duration Observation of Signals, Forward and Backward Linear Prediction, AR Lattice and ARMA Lattice – Ladder Filters, Wieners Filters for Filtering on Prediction. Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:explain the applications of digital filters
- LO 2:understand forward and backward linear prediction
- LO 3: explain how to predict different filters

UNIT-IV

DIGITAL SIGNAL PROCESSING ALGORITHMS: The Goertzel Algorithm, The Chirpz -Transform Algorithm, The Levinson – Durbin Algorithms, The Schur Algorithm, and other Algorithms, Computations of the DFT, Concept of Tunable Digital Filters.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:explain different types of algorithms
- **LO 2:**explain differences between types of algorithms.
- LO 3: understand computations of the DFT

UNIT-V

SIGNAL PROCESSING HARDWARE AND FFT ARCHITECTURES AND PROCESSORS:

Multipliers, Dividers, Different Forms of FIR Hardware, Multiplexing, DTTR, TDM to FDM Translator, Realization of Frequency Synthesizer. FFT Hardware Realization, Different FFT Architectures, Special FFT Processors, Convolves, Lincoln Laboratory FDP and the Compatible Computer Configurations.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:understand different forms of FIR hardware.
- LO 2:understand realization of frequency synthesizer
- LO 3: understand various computer configurations

UNIT-VI

APPLICATIONS OF DSP:Speech and DTMF Systems: Model of Speech Production, SpeechAnalysis –Synthesis System Vocoder Analyzers and Synthesizers, Linear Prediction of Speech and DTMF System.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand the model of speech productions

LO 2: explain applications of DSP

LO 3:explain linear prediction of speech

TEXT BOOKS:

- 1. Theory and Applications of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold, PHI.
- 2. Digital Signal Processing. Principles, Algorithms, and Applications by John G. Proakis and Dimitris G. Manolakis, PHI, 1997.

REFERENCE:

1. Digital Signal Processing, A Computer – Based approach, by Sanjit K. Mitra, Tata McGraw-Hill, 1998

Elective-I

APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASIC)

Credits: 3

Subject Code :MTVL – 1.3 I – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To prepare the student to be an entry-level industrial standard ASIC **CEO 2**: To give the student an understanding of issues and tools related to ASIC

CEO 3:To give the student an understanding of basics of System on Chip and Platform based design.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Architect ASIC library design
CO 2:Develop programmable ASIC logic cells
CO 3:Design I/O cells and interconnects
CO 4:Identify new developments in SOC and low power design.
CO 5:design cell design

UNIT- I

Introduction to ASICs – Types of ASICs, Design flow, Economics of ASICs, ASIC Cell Libraries, CMOS Logic, CMOS Design Rules, Logic Cells, I/O Cells, Cell Compilers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand different types of ASICs

LO 2: Explain CMOS Design Rules

UNIT- II

ASIC Library Design – Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Cell Design, Programmable ASICs, Programmable ASIC Logic Cells, Programmable ASIC I/O Cells, Programmable ASIC Interconnect, Programmable ASIC Design Software.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:Understand ASIC Library design

LO 2:Explain ASIC design Software

UNIT -III

Low-level Design Entry, Schematic Entry, Low-Level Design Languages, PLA Tools, EDIF, An overview of VHDL and Verilog, Logic Synthesis, Simulation. ASIC Construction, Floor Planning and Placement.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand overview of VHDL and VERilog

LO 2:explain the simulation of ASIC

UNIT- IV

CMOS System Core Studies: Dynamic Warp Processors: Introduction, The Problem, The Algorithm, A Functional Overview, Detailed Functional Specification, Structural Floor Plan, Physical Design, Fabrication, Hierarchical Layout And Design Of Single Chip 32 Bit CPU: Introduction, Design Methodology, Technology Updatability And Layout Verification.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain CMOS system core studies

LO 2:understand layouts of CMOS system

UNIT -V

Practical Realities and Ground Rules: Further Thoughts on Floor Plans/Layout, Floor Plan Layout of The Four Bit Processors, Input/output (I/O) Pads, "Real estate", Further Thoughts on System Delays, Ground Rules for Successful Design, Scaling of MOS Circuits.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand practical realities and ground rules

LO 2:explain ground rules of successful design.

TEXTBOOK:

1. Application Specific Integrated Circuits by J.S. Smith, Addison Wesley, 1997.

REFERENCES:

- 1. Basic VLSI Design : Systems and Circuits, Doublas A. Pucknell& Kamran Eshraghian, Prentice Hall of India Private Ltd., New Delhi, 1989.
- VLSI Design Techniques for analog and digital circuits, R.L. Geiger, P.E. Allen & N.R. Streder, McGraw Hill Int. 1990.

Elective-I

ADVANCED MICROPROCESSORS AND MICROCONTROLLERS

Credits : 3

Max. Marks :70

Sessionals :30

Subject Code: MTVL – 1.3 I – Semester CourseeducationalObjectives: The objectives of this course is

 $CEO\ 1$: Know the internal organization, addressing modes and instruction sets of 8086 processor

CEO 2: Know the various functional units of 8051 microcontroller

CEO 3:Understand embedded C and assembly language program by using 8051 Instruction sets and addressing modes.

CEO 4: Understand microcontroller based system design for various applications.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Develop an embedded C and ALP in 8051 microcontroller using the internal functional blocks for the given specification

CO 2:Explain microcontroller application and basic architecture of PIC,ARM and ATMEGA processors

CO 3: Describe the architecture and functional block of 8051 microcontroller

CO 4: Describe the architecture and functional block of 8051 microcontroller

CO 5: explain the internal organization, addressing modes and instruction sets of 8086 processor

Unit –I :

8086 / 8088 Microprocessor, Architecture and Addressing Modes. Instructions and assembly Language programming. Macro Assembler MASM and Advanced Programming.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain addressing modes of 8086

LO 2:understand the architecture of 8086

Unit –II:

Interrupts of 8086 / 8088 and DOS Interrupt 21h functions. Interfacing A/D converters to the PC and data acquisition. Interfacing D/A converters and waveform generation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain different types of interrupts

LO 2:understand interfacing of A/D converters

Unit – III:

80286, 80386, 80486 and Pentium Microprocessors. Motorola 68000, 68020 and 68030 Microprocessors.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain comparison between different types of processors **LO 2:**understand series of Motorola

Unit –IV: General Microcontrollers

Introduction to the 8051 and 8052 Microcontrollers, features, architectures, memory organization, addressing modes, instruction set, assembly programming, software development tools, parallel I/O ports, interrupts, timers/counters, serial communication, data and control transfer operations, serial data transmissions, programming and interfacing using 8051.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand the architecture of 8051

LO 2:explain interrupts of 8051

Unit -V: Atmel Microcontrollers

Introduction to Atmel microcontrollers (89CXX and 89C20XX), Architecture overview of Atmel 89C51, pin description of Atmel microcontrollers, using flash memory devices, Atmel 89CXX and Atmel 89C20XX, Applications of MCS-51 and Atmel 89C51 and 89C2051 microcontrollers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand overview of ATMEL microcontroller

LO 2:explain the pins of 89c51

Unit -VI: PIC Microcontrollers

An introduction to PIC microcontrollers, PIC 8 series and PIC 16 series microcontrollers and PIC family of microcontrollers (16C8X/7X, 16F84A, 12F50X and 16F8XX), architecture, instruction set, programming using assembly language and C languages of the PIC microcontrollers, interfacing PIC Microcontrollers to the other devices, applications of PIC microcontrollers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand overview of PIC

LO 2:explain assembly language and c Languages of PIC

Text Books:

- 1. Microprocessor and Interfacing by Douglas V. Hall, McGraw Hill International Edition, 1992.
- 2. The Intel Microprocessor 8086 / 8088, 80186, 80286, 80386 and 80486 by Barry B. Brey, PHI, 1998.

References:

- 1. Assembly Language Programming the IBM PC by Alan R. Miller, Sybex INC, 1987.
- 2. 68000 Microprocessors by Walter A. Tribel and Avtar Singh, PHI, 1991.
- 3. Microcontrollers –Theory and Applications –by Ajay V Deshnukh –TMH Publications.
- 4. The 8051 Microcontroller Architecture, Programming and Applications by Kenneth Ayala, Thomson Publishers

Elective-II

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

Credits : 3

Subject Code :MTVL – 1.4 I – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: Familiarization of various complex programmable Logic devices of different families.

CEO 2:To study Field programmable gate arrays and realization techniques **CEO 3:**To study different case studies using one hot design methods.

CourseOutcomes:At the completion of the course the student will be able to

CO 1:Acquire Knowledge about various architectures and device technologies of PLD's

CO 2:Comprehend FPGA Architectures.

CO 3:Describe FSM and different FSM techniques like petrinets& different case studies.

CO 4:Comprehends FSM Architectures and their applications.

CO 5:Analyze System level Design and their application for Combinational and Sequential Circuits.

UNIT –I

Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA – Features, Architectures, Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain different types of PLDS

LO 2: understand the applications of PLDS

UNIT-II

CPLDs: Complex Programmable Logic Devices: Altera series – Max 5000/7000 series and Altera FLEX logic- 10000 series CPLD, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice PLSI's architectures – 3000 series – Speed performance and in system programmability.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain different types of CPLDS

LO 2:understand speed performance and in system programmability

UNIT – III

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow,technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:Explain design flow of FPGA

LO 2:understand case studies of FPGA

UNIT-IV

Finite State Machines (FSM): Top Down Design, State Transition Table , State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine. Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petri nets for state machines-Basic concepts and properties, Finite State Machine-Case study.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain state assignment of FSM

LO 2:understand case studies of FSM

UNIT- VI

Design Methods and System Level Design: One –hot design method, Use of ASMs in one-hot design method, Applications of one hot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers.Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:use of ASM in one hot design method

LO 2:explain design tools for FPGA & ASIC

UNIT – VIII

Case studies: Design considerations using CPLDs and FPGAs of parallel adder cell, paralleladder sequential circuits, counters, multiplexers, parallel controllers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain case studies of CPLDS & FPGA

LO 2: understand sequential circuits

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.

2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.

3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan& S. Mourad, 1994, Prentice Hall.

2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose, Z.G.Vranesic, 2007, BSP.

Elective-II VHDL MODELLING OF DIGITAL SYSTEMS

Credits: 3

Subject Code :MTVL – 1.4 I – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To gain an in-depth understanding of VHDL and to realize different circuits using it both sequential and combinational.

CEO 2:To learn the concept of memories and how they are designed using VHDL.

CEO 3:To gain an understanding of applications of VHDL in PLDs and Field Programmable Logic Arrays(FPGAs).

CourseOutcomes: At the completion of the course the student will be able to

CO 1:explain VHDL as a programming language.

CO 2:Design the combinational and sequential logic circuits using VHDL.

CO 3:design Programmable logic devices(PLDs) and Networks of Arithmetic operations.

CO 4: understanding of applications of VHDL in PLDs

CO 5:Gain proficiency with VHDL software package and utilize software package to solve problems on a wide range of digital logic circuits.

UNIT I

INTRODUCTION

An Overview Of Design Procedures Used For System Design Using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples Using Commercial PC Based On VHDL Elements Of VHDL Top Down Design With VHDL Subprograms. Controller Description VHDL Operators.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand overview of CAD tools

LO 2:explain top down design with VHDL

UNIT II

BASIC CONCEPT IN VHDL

Characterizing Hardware Languages, Objects And Classes, Signal Assignments, Concurrent And Sequential Assignments. Structural Specification Of Hardware: Parts Library Wiring Of Primitives, Wiring Interactive

Networks, Modeling A Test Bench Binding Alternative Top Down Wiring.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain basic concepts in VHDL

LO 2:understand library writing of primitives

UNIT III

DESIGN ORGANIZATIN AND PARAMETERIZATION

Definition And Usage If Subprograms, Packaging Parts And Utilities, Design Parametrization, Design Configuration, Design Libraries, Utilities For High –Level Descriptions-Type Declaration And Usage, VHDL Operators, Subprogram Parameter Types And Overloading, Other Types And Type Related Issues, Predefined Attributes, User Defined Attributes, Packing Basic Utilities.

Learning Outcomes: At the end of the unit, the student will be able to

- **LO 1:**explain design parametrization for HLL
- LO 2:understand user defined attributes

UNIT IV

DATA FLOW DESCRIPTION IN VHDL

Multiplexing And Data Selection, State Machine Description, Open Collector Gates, Three State Bussing AGeneral Data Flow Circuit, Updating Basic Utilities. Behavioral Description Of Hardware: Process Statement Assertion Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain data flow circuit

LO 2:understand sequential wait statements

UNIT V

CPU MODELLING FOR DESCRIPTION IN VHDL

Parwan CPU, Behavioral Description OfParawan, Bussing Structure, Data Flow Description Test Bench For The Parwan CPU. A More Realistic Parwan. Interface Design And Modeling. VHDL As A Modelling Language.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain different types of modelling in VHDL

LO 2:understand PARWAN

TEXT BOOKS:

1. Z.NAWABI : VHDL Analysis And Modelling Of Digital Systems. (2/E), Mcgraw Hill, (1998)

REFERENCE:

1. PERRY : VHDL, (3/E) Mcgraw Hill 10

Elective –II

ELECTRONIC DESIGN AUTOMATION TOOLS

Credits: 3

Max. Marks :70

Sessionals :30

Subject Code :MTVL – 1.4 I – Semester CourseeducationalObjectives: The objectives of this course is

 $CEO\ 1:$ This Course gives an idea about the tools and techniques for integrated circuit design

CEO 2:This course deals with Functional design and verification, Frontend, Back-end IC design flow and tools, Mixed signal design flow for integrated circuit design. **CEO 3:**Capability in Microelectronics design and Implementation using Electronic Design Automation (EDA) tools.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Design hardware/software system models in a suitable system-level modeling language, such as SystemC.

CO 2: Use suitable heuristics to partition functional models into hardware and software components.

CO 3:Construct models for expressing functionalities of a system with appropriate models of computation and optimize such models for efficient simulation.

CO 4:Compare the complexity and efficiency of various algorithms for high-level synthesis from system models and design programs to implement such algorithms.

CO 5:Express semantics of various modeling languages using formal notations and techniques for expressing models of computation.

UNIT I

IMPORTANT CONCEPTS IN VERILOG:

Basics Of Verilog Language, Operators, Hierarchy, Procedures AndAsignments, Timing Controls And Delay. Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, other Verilog Features.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand basics of Verilog language

LO 2:explain altering parameters

UNIT II

SYNTHESIS AND SIMULATION USING HDLS:

Verilog Logic Synthesis. VHDL Synthesis, And And Logic MemorySynthesis,FSMSynthesis,Memory Synthesis, Performance-Driven Synthesis. Simulation-Types Of Simulation, Logic Systems Working Of Logic Simulation, Cell Models, Delay Models State Timing Analysis, Formal Verification, Switch-Level Simulation Transistor-Level Simulation. CAD Tools For Synthesis And Simulation Model sim And Leonardo Spectrum(Exemplar).

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand VHDL and Logic synthesis

LO 2:explain synthesis and simulation model sim
UNIT III

TOOLS FOR CIRCUIT DESIGN AND SIMULATION USING PSPICE:

Pspice Models For Transistors, A/D & D/A Sample And Hold Circuits Etc, And Digital System Building Blocks, Design And Analysis Of Analog And Digital Circuits Using PSPICE.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand PSPICE models for transistors

LO 2: design analog and digital circuits using PSPICE

UNIT IV

AN OVER VIEW OF MIXED SIGNAL VLSI DESIGN:

Fundamentals Of Analog And Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration To CAE Environments, Analyses Of Analog Circuits Eg.A/D, D/A Converters, Up And Down Converters, Companders Etc.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain mixed signal simulator configurations

LO 2:explain up and down converters

UNIT V

TOOLS FOR PCB DESIGN AND LAYOUT:

An Overview Of High Speed PCB Design, Design Entry, Simulation And Layout Tools For PCB. Introduction ToOrcad PCB Design Tools.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain overview of high speed PCB design

LO 2:explain orcad PCB tools

TEXTBOOKS

- 1. J.Bhaskar, A Verilog Primer, BSP, 2003.
- 2. J.Bhaskar, A Verilog HDL Synthesis BSP, 2003
- 3. M.H.RASHID:SPICE FOR Circuits And Electronics Using PSPICE (2/E)(1992) Prentice Hall.

REFERENCES

Semester-I

- 1. ORCAD: Technical Reference Manual .Orcad, USA.
- 2. SABER: Technical Reference Manual, Analogy Nic, USA.
- 3. M.J.S.SMITH : Aplication-Specific Integrated Circuits(1997). Addison Wesley
- 4. J.Bhaskar, A VHDL Synthesis Primer, BSP, 2003.

RESEARCHMETHODOLOGY AND IPR

Credits: 2 Exam Marks: 70 Subject Code: MTVL – 1.5 Sessional: 30

CourseeducationalObjectives: The objectives of this course is

 $CEO\ 1:$ To give an overview of the research methodology and explain the technique of defining a research problem

CEO 2: To explain the functions of the literature review in research

CEO 3:To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review

CEO 4:To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Understand research problem formulation.

CO 2:Analyze research related information

CO 3:Follow research ethics

CO 4:Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.

CO 5:Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Unit 1: Meaning of research problem, Sources of research problem, Criteria

Characteristics of a good research problem, Errors in selecting a research problem, Scope

and objectives of research problem. Approaches of investigation of solutions for research

problem, data collection, analysis, interpretation, Necessary instrumentations.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain research problem

LO 2: understand errors in selecting research problem

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics,

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand plagarism

LO 2:explain research ethics

Unit 3: Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand technical writing

LO 2:explain format of research proposal

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:understand patents, designs
- LO 2:understand international scenario.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Learning Outcomes: At the end of the unit, the student will be able to LO 1: understand patent rights LO 2:understand geographical indications

Unit 6: New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Learning Outcomes: At the end of the unit, the student will be able to LO 1:understand administration in patent systems LO 2:explain case studies in IPR & IITs

REFERENCES:

- 1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science
- 2. & engineering students'"
- 3. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- 4. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
- 5. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
- 6. Mayall, "Industrial Design", McGraw Hill, 1992.
- 7. Niebel, "Product Design", McGraw Hill, 1974.
- 8. Asimov, "Introduction to Design", Prentice Hall, 1962.
- 9. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New
- 10. Technological Age", 2016.
- 11. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

AUDIT COURSE 1&2 ENGLISH FOR RESEARCH PAPER WRITING

Subject Code: MTVL – 1.6&2.5 Semester-I&II

Credits: 0 Sessional: 100

1. Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

2. Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

3. Review of the Literature, Methods, Results, Discussion, Conclusions, the Final Check.

4. Key skills are needed when writing a Title, key skills are needed when writing an abstract, key kills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

5. Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, and skills are needed when writing the Conclusions

6. Useful phrases, how to ensure paper is as good as it could possibly be the first- time Submission.

REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)

2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM.

Highman'sbook .

 Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

AUDIT COURSE 1&2 DISASTER MANAGEMENT

Subject Code: MTVL – 1.6&2.5 Semester-I&II Credits: 0 Sessional: 100

1 **Introduction:** Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

2 **Repercussions Of Disasters And Hazards**: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Manmade disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

3 **Disaster Prone Areas In India :**Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides AndAvalanches; Areas Prone To Cyclonic And Coastal Hazards With Special ReferenceTo Tsunami; Post-Disaster Diseases And Epidemics

4 Disaster Preparedness And Management Preparedness: Monitoring Of Phenomena

Triggering A Disaster Or Hazard;Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological AndOther Agencies, Media Reports: Governmental And Community Preparedness.

5 **Risk Assessment** Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And NationalDisaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation InRisk ssessment And Warning, People's Participation In Risk Assessment. Strategiesfor Survival.

6 **Disaster Mitigation** Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends InMitigation. Structural Mitigation And Non-Structural Mitigation, Programs OfDisaster Mitigation In India.

REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "New

Royal book Company.

2. Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall

Of India, New Delhi.

3. Goel S. L., Disaster Administration And Management Text And Case Studies", Deep &Deep

Publication Pvt. Ltd., New Delhi.

AUDIT COURSE 1&2

SANSKRIT FOR TECHNICAL KNOWLEDGE

Subject Code: MTVL – 1.6&2.5

Semester-I&II

Credits: 0 Sessional: 100

1 Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

2 Order

Introduction of roots

Technical information about Sanskrit Literature

3 Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

REFERNCES:

1. "Abhyaspustakam" - Dr. Vishwas, Samskrita-Bharti Publication, New Delhi

2. "Teach Yourself Sanskrit" PrathamaDeeksha-VempatiKutumbshastri, Rashtriya Sanskrit

Sansthanam, New Delhi Publication

3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

AUDIT COURSE 1&2 VALUE EDUCATION

Subject Code: MTVL – 1.6&2.5 Semester-I&II

Credits: 0 Sessional: 100

1 Values and self-development -Social values and individual attitudes. Work ethics. Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements 2 Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline 3 Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature 4 Character and Competence – Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. **REFERNCES:**

1 Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

AUDIT COURSE 1&2

CONSTITUTION OF INDIA

Subject Code: MTVL – 1.6&2.5 Semester-I&II

1 History of Making of the Indian Constitution:

Credits: 0 Sessional: 100

History Drafting Committee, (Composition& Working) 2Philosophy of the Indian Constitution: Preamble Salient Features **3** Contours of Constitutional Rights & Duties: **Fundamental Rights Right to Equality** Right to Freedom **Right against Exploitation** Right to Freedom of Religion Cultural and Educational Rights **Right to Constitutional Remedies Directive Principles of State Policy** Fundamental Duties. **4 Organs of Governance:** Parliament Composition **Qualifications and Disqualifications** Powers and Functions Executive President

Governor

Council of Ministers

Judiciary, Appointment and Transfer of Judges, Qualifications

Powers and Functions

5 Local Administration:

District's Administration head: Role and Importance,

Municipalities: Introduction, Mayor and role of Elected Representative, CEO of

Municipal Corporation.

Pachayati raj: Introduction, PRI: ZilaPachayat.

Elected officials and their roles, CEO ZilaPachayat: Position and role.

Block level: Organizational Hierarchy (Different departments),

Village level: Role of Elected and Appointed officials,

Importance of grass root democracy

6Election Commission:

Election Commission: Role and Functioning.

Chief Election Commissioner and Election Commissioners.

State Election Commission: Role and Functioning.

Institute and Bodies for the welfare of SC/ST/OBC and women.

REFERNCES:

- 1. The Constitution of India, 1950 (Bare Act), Government Publication.
- 2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
- 3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
- 4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AUDIT COURSE 1&2 PEDAGOGY STUDIES

Subject Code: MTVL – 1.6&2.5 Semester-I&II Credits: 0 Sessional: 100

1 Introduction and Methodology:

Aims and rationale, Policy background, Conceptual framework and terminology

Theories of learning, Curriculum, Teacher education.

Conceptual framework, Research questions.

Overview of methodology and Searching.

2Thematic overview: Pedagogical practices are being used by teachers in formaland informal

classrooms in developing countries.Curriculum, Teacher education.

3 Evidence on the effectiveness of pedagogical practices

Methodology for the in depth stage: quality assessment of included studies.

How can teacher education (curriculum and practicum) and the school curriculum and

guidance materials best support effective pedagogy?

Theory of change.

Strength and nature of the body of evidence for effective pedagogical practices.

Pedagogic theory and pedagogical approaches.

Teachers' attitudes and beliefs and Pedagogic strategies.

4 Professional development: alignment with classroom practices and follow support Peer support.

Support from the head teacher and the community.

Curriculum and assessment.

Barriers to learning: limited resources and large class sizes.

5 Research gaps and future directions

Research design

Contexts

Pedagogy

Teacher education

Curriculum and assessment

Dissemination and research impact.

REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31

(2): 245-261.

2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of

Curriculum Studies, 36 (3): 361-379.

3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education

research project (MUSTER) country report 1. London: DFID.

4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of

basicmaths and reading in Africa: Does teacher preparation count? International Journal

Educational Development, 33 (3): 272–282.

5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education.

Oxford and Boston: Blackwell.

6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.

7. www.pratham.org/images/resource%20working%20paper%202.pdf.

AUDIT COURSE 1&2

STRESS MANAGEMENT BY YOGA

Subject Code: MTVL – 1.6&2.5 Semester-I&II

Credits: 0 Sessional: 100

- 1 Definitions of Eight parts of yog. (Ashtanga) 8
- 2 Yam and Niyam.

Do's and Don't's in life.

- i) Ahinsa, satya, astheya, bramhacharya and aparigraha
- ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan
- 3 Asan and Pranayam
 - i) Various yog poses and their benefits for mind & body
 - ii)Regularization of breathing techniques and its effects-Types of pranayam

REFERENCES

1. 'Yogic Asanas for Group Tarining-Part-I" :Janardan Swami YogabhyasiMandal, Nagpur

2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata.

AUDIT COURSE 1&2

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

Credits: 0

Subject Code: MTVL – 1.6&2.5 Sessional:100 Semester-I&II 1 Neetisatakam-Holistic development of personality Verses- 19,20,21,22 (wisdom) Verses- 29,31,32 (pride & heroism) Verses- 26,28,63,65 (virtue) Verses- 52,53,59 (dont's) Verses- 71,73,75,78 (do's) 2 Approach to day to day work and duties. ShrimadBhagwadGeeta: Chapter 2-Verses 41, 47,48, Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5, 13, 17, 23, 35, Chapter 18-Verses 45, 46, 48. 3 Statements of basic knowledge. ShrimadBhagwadGeeta: Chapter2-Verses 56, 62, 68 Chapter 12 - Verses 13, 14, 15, 16, 17, 18 Personality of Role model. ShrimadBhagwadGeeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, Chapter 4-Verses 18, 38,39 Chapter18 – Verses 37,38,63 REFERENCES 1. "Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication

Department),

Kolkata

2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

HDL PROGRAMMING LABORATORY

Credits: 2

Subject Code: MTVL – 1.7 I – Semester Max. Marks: 100

CourseeducationalObjectives: The objectives of this course is

CEO 1: To gain an in-depth understanding of VHDL and to realize different circuits using it both sequential and combinational.

CEO 2:To learn the concept of memories and how they are designed using VHDL.

CEO 3:To gain an understanding of applications of VHDL in PLDs and Field Programmable Logic Arrays(FPGAs).

CourseOutcomes:At the completion of the course the student will be able to

CO 1:explain VHDL as a programming language.
CO 2:Design the combinational and sequential logic circuits using VHDL.
CO 3:design Programmable logic devices(PLDs) and Networks of Arithmetic operations.
CO 4:understanding of applications of VHDL in PLDs

CO 4: understanding of applications of VHDL in PLDs **CO 5:**Gain proficiency with VHDL software package and utilize software package to solve problems on a wide range of digital logic circuits.

- 1. Basic Gates
- 2. Adders
- 3. Subtractors
- 4. Full Adder Using Two Half Adders
- 5. Decoders
- 6. 4 Bit Binary Adder
- 7. Multiplexer
- 8. Encoder
- 9. Demultiplexers
- 10. Comparators
- 11. Flip flops
- 12. Counters
- 13. Shift registers
- 14. Mealy & Moore Machine for sequence detector

15. Implementation of ALU

16. RAM(4X4)

ANALOG IC DESIGN LAB

Credits: 2

Subject Code: MTVL – 1.7 I – Semester Max. Marks: 100

CourseeducationalObjectives: The objectives of this course is

CEO 1: To provide in-depth understanding of the analog integrated circuit and building blocks

CEO 2: To provide a basic idea on mixed signal IC design

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Able to carry out research and development in the area of analog and mixed signal IC design.

CO 2:To be well versed with the MOS fundamentals, small signal models and analysis of MOSFET based circuits.

CO 3:Able to analyze and design analog circuits such as Differential Amplifier, OP-AMP, Current mirrors, Biasing circuits

CO 4:Able to analyze and design mixed mode circuits such as Comparator, ADCs, DACs, PLL.

CO 5:Solve practical and state of the art analog IC design problems to serve VLSI industries.

Design and evaluate the following analog circuits

- 1. Analysis of CE, CC and CB amplifiers and their frequency response
- 2. Single transistor amplifiers using NMOS (CD, CS and CG)
- 3. Current sinks
- 4. Current sources
- 5. Current mirrors
- 6. Differential amplifier
- 7. Two stage Operational amplifier design

DIGITAL SYSTEM DESIGN

Credits : 3

Subject Code :MTVL -2.1 II – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To acquire the basic knowledge of digital logic levels and application of knowledge to understand digital electronics circuits.

CEO 2:To prepare students to perform the analysis and design of various digital electronic circuits

CourseOutcomes: At the completion of the course the student will be able to

CO 1:explain and distinguish procedures and methods in the field of complex digital system design

CO 2:apply design methods for new applications

CO 3: analyze and breakdown a complex digital system

CO 4: design and develop a VHDL model of a system

CO 5: design and develop a complex digital system based on ASIC

UNIT – I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand ASM charts

LO 2: understand hardware description language

UNIT – II

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs. **Learning Outcomes:** At the end of the unit, the student will be able to

LO 1:understand ROM & PLAs

LO 2:explain design using CPLD, fpgas

UNIT – III

FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transitionand intermittent faults. TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand different types of faults

LO 2: explain path sensitization

UNIT – IV

TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transitioncount testing, Signature analysis and testing for bridging faults.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand PODEM

LO 2: explain signature analysis for bridging circuits

UNIT – V

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and faultdetection experiment. Machine identification, Design of fault detection experiment.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand state identification and detection

LO 2:design of fault detection experiment

UNIT – VI

PROGRAMMING LOGIC ARRAYS AND ASYNCHRONOUS SEQUENTIAL MACHINE: Design using PLA's, PLA minimization and PLA folding. Fault models, Testgeneration and Testable PLA design. Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:design of PLA

LO 2:understand testing of PLA design

TEXT BOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)

2. N. N. Biswas – "Logic Design Theory" (PHI)

3. NolmanBalabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition

2004.

REFRENCES:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications

2. Charles H. Roth Jr. - "Fundamentals of Logic Design".

3. Frederick. J. Hill & Peterson - "Computer Aided Logic Design" - Wiley 4th Edition. 4

ALGORITHMS FOR VLSI DESIGN AUTOMATION

Credits : 3

Max. Marks :70

Sessionals :30

Subject Code :MTVL – 2.2 II – Semester

CourseeducationalObjectives: The objectives of this course is

CEO 1: Attain mastery in applying VLSI concepts to Engineering problems so as to meet the need of the industry, teaching, higher education or research.

CEO 2:To understand other process steps like etching, implantation and metallization and their implications.

CEO 3:To understand the semiconductor materials, devices and technology historical evaluations

CEO 4:To explain the oxidization process and quality measures in the fabrication

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Identify the various design methodologies

CO 2::Describe the combinational optimization

CO 3::Understand the modeling & simulation

CO 4: Apply logic synthesis and verification

CO 5:Assess the physical design automation.

UNIT- I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand design methodologies

LO 2:explain graph theory

UNIT- II

GENERAL PURPOSE METHODS FOR COMBINATIONAL

OPTIMIZATION:Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, LocalSearch, Simulated Annealing, Tabu search, Genetic Algorithms, Layout Compaction, Placement, Floorplanning and Routing Problems, Concepts and Algorithms.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand programming tools

LO 2:explain different types of algorithms

UNIT-III

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch levelmodeling and simulation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:observe the simulation of gate level modeling

LO 2:explain level modeling

UNIT-IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis, Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations. **Learning Outcomes:** At the end of the unit, the student will be able to

LO 1:explain two level logic synthesis

LO 2:understand scheduling algorithms

UNIT –V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Designcycle for FPGA's partitioning and Routing for segmented and staggered models. **Learning Outcomes:** At the end of the unit, the student will be able to

LO 1:understand FPGA technologies

LO 2:explain routing

UNIT –VI

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physicaldesign cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand physical design

LO 2:explain topological routing

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, John wiley& Sons (Asia) Pvt.Ltd. 1999.

2. Algorithms for VLSI Physical Design Automation, 3rd edition, NaveedSherwani, Springer International Edition, 2005

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993

2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

Elective III LOW POWER VLSI DESIGN

Credits: 3

Subject Code: MTVL – 2.3 II – Semester Max. Marks: 70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: This course addresses a profound analysis on the development of the CMOS & Bi-CMOS digital circuits for a low voltage low power environment

CEO 2:To study the concepts of device behavior and modeling

CEO 3: To study the concepts of low voltage, low power logic circuits

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Capability to recognize advanced issues in VLSI systems, specific to the deep-submicron silicon technologies.

CO 2:Students able to understand deep submicron CMOS technology and digital CMOS design styles.

CO 3: To design chips used for battery-powered systems and highperformance circuits

CO 4:Explain the equations, approximations and techniques available for deriving a device model with specified properties

CO 5:Explore and improvise on the latest techniques used for designing powerefficient logic gates, latches, and flip-flops

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low powerdesign, limitations, Silicon-on-Insulator.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain low power low voltage design

LO 2:explain silicon-on-insulator

UNIT II

MOS/BiCMOS PROCESSES: Bi CMOS processes, Integration and Isolationconsiderations, Integrated Analog/Digital CMOS Process. Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand BICMOS process

LO 2:explain deep submicron processes

UNIT III

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand device behavior modeling

LO 2: explain experimental characterization of MOS devices

UNIT IV

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates.Performance evaluation.

Learning Outcomes: At the end of the unit, the student will be able to

- **LO 1:**explain cmos and bicmos logic gates
- LO 2:understand performance evaluation of CMOS

UNIT V

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of

advancedBiCMOS Digital circuits. ESD-free Bi CMOS, Digital circuit operation and comparative Evaluation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand low voltage low power logic circuits

LO 2:explain digital circuit operation

UNIT VI

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flopsquality measures for latches and Flip flops, Design perspective.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand latches & flipflops

LO 2:explain design perspective

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES

- 1. Digital Integrated circuits, J.Rabaey PH. N.J 1996
- 2. CMOS Digital ICs sung-moKang and yusufleblebici 3rd edition TMH2003 (chapter 11)
- 3. VLSI DSP systems, Parhi, John Wiley & sons, 2003 (chapter 17)
- 4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

Elective-III

WIRELESS COMMUNICATIONS AND NETWORKS

Credits: 3

Subject Code :MTVL – 2.3 II – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To enable students to acquire in-depth knowledge in the field of wireless communication technology with an ability to integrate existing and new knowledge with the advancement of the technology.

CEO 2:To develop students to critically analyze the problems in the field of wireless communication technology and find optimal solution.

CEO 3:To train students to conduct research and experiments by applying appropriate techniques and tools with an understanding of the limitations for sustainable development of society

CEO 4:To prepare students to act as a member and leader of the team to contribute positively to manage projects efficiently in the field of wireless communication technology.

CourseOutcomes:At the completion of the course the student will be able to

CO1:Demonstrate their understanding on functioning of wireless communication system and evolution of different wireless communication systems and standards.

CO2:Compare different technologies used for wireless communication systems.

CO3:Explain the architecture, functioning, protocols, capabilities and application of various wireless communication networks.

CO4:Demonstrate an ability explain multiple access techniques for Wireless Communication

CO5:Demonstrate an ability to evaluate design challenges, constraints and security issues associated with Ad-hoc wireless networks.

UNIT -I

WIRELESS COMMUNICATION AND SYSTEM FUNDAMENTALS: Introduction toWireless Communication Systems, Examples of Wireless Communications, Comparisons of Common Wireless Communication Systems, Trends in Cellular Radio and Personal Communications, Cellular Concepts, Frequency Reuse, Handoff Strategies, Interference and System Capacity, Trucking and Grade Of Service, Improving Coverage & Capacity In Cellular Systems.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand wireless communications

LO 2:explain fundamentals of wireless communication

UNIT-II

MULTIPLE ACCESS TECHNIQUES FOR WIRELESS COMMUNICATION: FDMA,TDMA, SSMA (FHMA/CDMA/Hybrid Techniques) SDMA Technique (As Applicable to Wireless Communications), Packet Radio Access Protocols, CSMA Protocols, Reservation Protocols, Capture Effect in Packet Radio, Capacity of Cellular Systems.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain multiple access techniques

LO 2:understand packet transmission

UNIT-III

WIRELESS NETWORKING: Introduction, Differences Between Wireless and FixedTelephone Networks, Traffic Routing in Wireless Networks, Circuit Switching, Packet Switching, The X.25 protocol.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain wireless networking

LO 2:understand various protocols

UNIT-IV

Wireless Data Services, Cellular Digital Packet Data (CDPD), Advanced Radio Data Information Systems (ARDIS), RAM Mobile Data (RMD), Common Channel Signaling (CCS), Broad Band ISDN and ATM, Signaling System .No.7 (SS7), Network Services Part (NSP), SS7 User Part, Signaling Traffic in SS7, SS7 Services, Performance of SS7.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain data services

LO 2:explain signaling systems

UNIT-V

MOBILE IP AND WIRELESS APPLICATION PROTOCOL: Mobile IP Operation of Mobile IP, Co-located Address, Registration, Tunneling, WAP Architecture, Overview, WML Scripts, WAP Service, WAP Session protocol, Wireless Transaction, Wireless Datagram, Infrared LAN's, Spread Spectrum LAN's, Narrowband Microwave LAN's, IEEE 802 Protocol Architecture, IEEE 802 Architecture and Services, 802. 11 Medium Access Controls, 802.11 Physical Layers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain mobile IP concepts

LO 2:explain WAP services

UNIT-VI

BLUE TOOTH AND MOBILE DATA NETWORKS: Overview, Radio Specification, Baseband Specification, Links Manager Specification, Logical Link Control and Adaptation Protocol, Introduction to WLL Technology, Introduction, and Data Oriented CDPD Network, GPRS and Higher Data Rates, Short Messaging Service in GSM, Mobile Application Protocol.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain Bluetooth transmission

LO 2:Explain mobile data network

TEXT BOOKS:

- 1. Wireless communication and Networking -William Stallings, PHI, 2003
- 2. Wireless Communications, Principles, Practice Theodore, S. Rappaport, PHI, 2nd Edition, 2002.

REFERENCES:

- 1. Wireless Digital Communications-Karnilofeher, PHI, 1999.
- 2. Principles of Wireless Networks Kavehpahlaven and P.Krishna Murthy, Pearson Education, 2002

Elective-III

RF AND MICROWAVE INTEGRATED CIRCUITS

Credits : 3

Subject Code :MTVL – 2.3 II – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To provide basic information on the RF circuit design

CEO 2: To familiar with RF CAD software to design linear and non-linear RF circuits

CEO 3: To design narrow and broadband RF circuits

CEO 4:To understand the difference between transient and harmonic balance analysis

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Understand RF circuits, devices, and system.

CO 2: Understand design of RF & Microwave Integrated Circuit.

CO 3:Solve problems related to it

CO 4:Analyze the RF & microwave circuits using various numerical techniques.

CO 5:Describe some basic properties of different radio architectures. Explain the applications of RF & MIC.

UNIT-I

Analysis and Design of RF and Microwave Lines – Review of Transmission Lines, Parallel Plate Transmission Lines, Low -Frequency Solution, High Frequency Solution,

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand analysis of RF and microwave lines

LO 2:understand high frequency solutions

UNIT-II

Strip Line And Micro Strip Transmission Lines, Low Frequency Solution, High Frequency Properties Of Micro Slot Line, Co Planer Wave Guides, Spiral Inductors – Capacitors.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain strip line transmission lines

LO 2:explain low frequency solution

UNIT-III

Microstrip/Strip line Based Filters. Resonators, Plane Shifters, Micro Strip Based Gyrators, Circulators And Isolators, Directional Couplers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand resonators

LO 2:explain directional couplers

UNIT-IV

Microwave Active Devices – Microwave Transistors, GaAs FETS (Structures, Equivalent Circuit), Low Noise Amplifiers, Power Amplifiers, Oscillators, Detect5ors, Mixers, Modulators and Switches.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain microwave active devices

LO 2:understand low noise amplifiers

UNIT-V

Technology of MICS: Deposition Techniques – Vacuum Evaporation – Vacuum Sputtering Ion Planting. MBE (molecular Beam Epitaxy) – Photo Lithography, Mask Preparation, Thick Film Technology, GaAs Technology.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain technology of MICS

LO 2:understand photolithography

UNIT-VI

MIC Packaging: Component Attachment, Bonding Techniques, Solder Reflow Techniques, Input/Output Terminations, Testing.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain MIC packaging

LO 2:understand I/O terminations

TEXT BOOKS:

- 1. Microwave Engineering Prof. G.S.N Raju, I.K. International Publication.
- 2. I.Kneppo and J. Fabian, "Microwave Integrated Circuit", London: Chapman & Hall, (1994).
- 3. M.W.Medley, "Microwave and RF circuit: Analysis, Synthesis and Design", Artech House, (1993).

REFERENCES:

- 1. R.Goyal, "Monolithic Microwave Integrated Circuit: Technology & Design", Artech House, (1989).
- 2. Y.Konishi, "Microwave Integrated Circuit", Dekker, New York: Marcel Dekker, (1991).

Elective-IV

MICROCONTROLLERS AND EMBEDDED SYSTEMS

Credits: 3

Subject Code :MTVL – 2.4 II – Semester Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To have knowledge about the basic working of a microcontroller system and its programming in assembly language.

CEO 2:To provide experience to integrate hardware and software for microcontroller applications systems.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Learn basic hardware of various microcontrollers.

CO 2:Assembly and programming concepts, jump and call instructions

CO 3:Hardware interfacing of microcontroller with led's, seven segment, sensors

CO 4:Introduction to 16-bit microcontrollers.

CO 5:Foster ability to understand the role of embedded systems in industry.

UNIT-1

INTRODUCTION: Embedded Systems overview, Design Challenge, ProcessorTechnology, IC Technology, Design Technology, Trade-offs.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain overview of embedded system

LO 2:understand trade offs

UNIT-II

CUSTOMSINGLE-PURPOSEPROCESSORS(HARDWARE):Introduction, Combinational logic, Sequential logic, Custom Single-Purpose ProcessorDesign, RT-Level Custom Single-Purpose Processor Design, Optimizing Custom Single-Purpose Processors.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain combinational logic

LO 2:explain sequential logic

UNIT-III

GENERAL PURPOSE PROCESSORS (SOFTWARE): Introduction, Basic Architecture,Operation, Programmer's view, Development Environment, Application-Specific Instruction-set Processors, Selecting a Microprocessor.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain general purpose processors

LO 2:understand development of processors

UNIT-IV

MEMORY: Introduction, Memory types, Memory Hierarchy and Cache, Advanced

MemoryInterfacing: Communication Basics, Memory Access, I/O addressing, Interrupts, DMA, Arbitration, Multilevel Architecture, Protocols.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain different memory types

LO 2:understand memory acess

UNIT-V

MICROCONTROLLERS: Review of 8051 Microcontroller Architecture &Programming.Peripherals: Timers, Counters and Watchdog Timers, UART, Pulse width Modulators, LCD Controllers, Stepper Motor Controllers, Analog to Digital Converters, Real-Time Clocks. Digital Camera Introduction, Specifications, Design.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand 8051 microcontroller

LO 2:explain real time clocks

UNIT-VI

STATE MACHINE AND CONCURRENT PROCESS MODELS: Introduction, ModelsVs Languages, Text Vs Graphics, Textual Languages Vs Graphical Languages, An Example, A Basic State Machine Model, FSM with Data Path Model, FSMD Using State Machines, Concurrent Process Model, Communication among Processes.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain state machines LO 2:explain fsm

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TEXT BOOKS:

- 1. Embedded System Design: A Unified Hardware/Software Introduction By Frank vahid / Tony Givargis John wiley& sons
- 2. The 8051 Microcontroller & Embedded Systems By Muhammad Ali Mazidi& Janice GillispieMazidi PHI

REFERENCES:

- 1. Embedded Systems Architecture, Programming and Design ByRajKamal TMH
- 2. Embedded Software PrinerBy Simon.
- The 8051 Microcontroller: Architecture, Programming & Applications. By Kenneth J.AyalaPenram International. 2ndedn.

Elective-IV

DIGITAL SYSTEMS TESTING AND TESTABLE DESIGN

Credits: 3

Max. Marks: 70

Sessionals: 30

Subject Code: MTVL – 2.4 II – Semester

CourseeducationalObjectives: The objectives of this course is

CEO 1: To expose the students, the basics of testing techniques for VLSI circuits and Test Economics.

CEO 2:This practical, hands-on course introduces digital logic design, systemlevel design using current state of the art in EDA tools used by professionals in VLSI field today

CourseOutcomes:At the completion of the course the student will be able to

CO 1:apply the concepts in testing which can help them design a better yield in IC design.

CO 2: tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.

CO 3:analyze the various test generation methods for static & dynamic CMOS circuits.

CO 4:identify the design for testability methods for combinational & sequential CMOS circuits. CO5: recognize the BIST techniques for improving testability.

CO 5:Ability to design and implement digital circuits under realistic constraints and conditions.

UNIT- I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) SIMULATIONS: Fundamentals, Modeling Digital Circuits at Logic Level, Register Leveland Structural Models. Levels of Modeling. Types of Simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain modeling digital circuits

LO 2:understand types of simulation

UNIT- II

FAULT MODELING: Logic fault models, Fault detection and redundancy, Faultequivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for combinational circuits.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain logic fault models

LO 2:understand single stuck and multiple stuck

UNIT- III

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation(ATPG/ATG) For SSFs In Combinational And Sequential Circuits ,Functional Testing With Specific Fault Models .Vector Simulation – ATPG Vectors ,Formats,

Compaction And Compression ,Selecting ATPG Tool.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain test pattern

LO 2:understand vector simulation

UNIT- IV

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan ArchitecturesAnd Testing – Controllability And Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells For Scan Design. Board Level And System Level DFT Approaches.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand testability trade-offs

LO 2:explain boundary scan

UNIT- V

BOUNDARY SCANS STANDARDS AND BIST: Compression Techniques – DifferentTechniques, Syndrome Test And Signature Analysis, BIST Concepts And Test Pattern Generation. Specific BIST Architectures CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts And Design for Self-Test at Board Level.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain BIST concepts

LO 2:understand BIST architectures

UNIT- VI

MEMORY BIST (MBIST): Memory Test Architectures And Techniques – Introduction to Memory Test, Types Of Memories And Integration, Embedded Memory Testing Model, Memory Test Requirements for MBIST, Brief Ideas on Embedded Core Testing, Introduction to Automatic In Circuit Testing (ICT), JTAG Testing Features.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain memory test architectures

LO 2:understand embedded memory testing model

TEXT BOOKS:

- 1. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House,2001
- 2. Alfred Crouch, Design for Test for Digital ICs and Embedded core systems, Prentice Hall.

REFERENCES:

1. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing ,Prentice Hall,Englehood Cliffs,1998

Elective-IV

DSP PROCESSORS AND ARCHITECTURES

Credits: 3

Subject Code: MTVL – 2.4 II – Semester Max. Marks: 70 Sessionals: 30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To give an exposure to the various fixed point & a floating point DSP architectures and to develop applications using these processors.

CEO 2:Design and implement signal processing modules in DSPs

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Recognize the fundamentals of fixed and floating point architectures of various DSPs.

CO 2:Learn the architecture details and instruction sets of fixed and floating point DSPs

CO 3:Illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.

CO 4:Analyze and learn to implement the signal processing algorithms in DSPs **CO 5:**Learn the DSP programming tools and use them for applications

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain digital signal processing system

LO 2:understand DFT & FFT

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: explain computational accuracy in DSP

LO 2:explain D/A conversion errors

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES AND EXECUTION

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing, Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain DSP building blocks

LO 2:explain pipelining and performance

UNIT IV

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand TMS320C54XX

LO 2:explain addressing modes

UNIT V

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS AND FFT ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing, An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain FIR filters

LO 2:explain Adaptive filters

UNIT VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain bus interfacing models

LO 2:Understand memory interfacing

TEXT BOOKS:

- 1. Digital Signal Processing Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
- 2. DSP Processor Fundamentals, Architectures & Features Lapsley et al. S. Chand & Co, 2000.

REFERENCES:

- 1. Digital Signal Processors, Architecture, Programming and Applications B. VenkataRamani and M.Bhaskar, TMH, 2004.
- 2. Digital Signal Processing Jonatham Stein, John Wiley, 2005.

Credits : 2

Max. Marks :100

Subject Code :MTVL –2.6 II – Semester

CourseeducationalObjectives: The objectives of this course is

CEO 1: To gain an in-depth understanding of VHDL and to realize different circuits using it both sequential and combinational.

CEO 2:To learn the concept of memories and how they are designed using VHDL.

CEO 3:To gain an understanding of applications of VHDL in PLDs and Field Programmable Logic Arrays(FPGAs).

CourseOutcomes: At the completion of the course the student will be able to

CO 1:explain VHDL as a programming language.
CO 2:Design the combinational and sequential logic circuits using VHDL.
CO 3:design Programmable logic devices(PLDs) and Networks of Arithmetic operations.
CO 4:understanding of applications of VHDL in PLDs
CO 5:Gain proficiency with VHDL software package and utilize software package to solve problems on a wide range of digital logic circuits.

Design and synthesize the following digital circuits using Verilog HDL and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

- 1. Basic Gates
- 2. Adders
- 3. Subtractors
- 4. Full Adder Using Two Half Adders
- 5. Decoders
- 6. 4 Bit Binary Adder
- 7. Multiplexer
- 8. Encoder
- 9. Demultipluxers
- 10. Comparators
- 11. Flip flops
- 12. Counters
- 13. Shift registers
- 14. Mealy & Moore Machine for sequence detector
15. Implementation of ALU

16. RAM (4X4)

MIXED SIGNAL SIMULATION LABORATORY

Credits : 2

Subject Code :MTVL –2.7 II – Semester Max. Marks :100

CourseeducationalObjectives: The objectives of this course is

CEO 1: To provide in-depth understanding of the analog integrated circuit and building blocks

CEO 2:To provide a basic idea on mixed signal IC design

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Able to carry out research and development in the area of analog and mixed signal IC design.

CO 2:To be well versed with the MOS fundamentals, small signal models and analysis of MOSFET based circuits.

CO 3:Able to analyze and design analog circuits such as Differential Amplifier, OP-AMP, Current mirrors, Biasing circuits

CO 4:Able to analyze and design mixed mode circuits such as Comparator, ADCs, DACs, PLL.

CO 5:Solve practical and state of the art analog IC design problems to serve VLSI industries.

By considering suitable complexity Mixed-Signal application based circuits (circuits consisting of both analog and digital parts), the students are required to perform the following aspects using necessary software tools.

- 1. Analog Circuits Simulation using Spice Software.
- 2. Digital Circuits Simulation using Xilinx Software.
- 3. Mixed Signal Simulation Using Mixed Signal Simulators.
- 4. Layout Extraction for Analog & Mixed Signal Circuits.
- 5. Parasitic Values Estimation from Layout.
- 6. Layout Vs Schematic.
 - a) Cmos Inverter
 - b) Two Input Cmos N Gate
 - c) Two Input Cmos Nor Gate
- 7. Net List Extraction.
- 8. Design Rule Checks.
 - a) Full Custom Layout of Inverter
 - b) Full Custom Layout of two input NAND

MTVL2.7 Mixed Signal Simulation LAB

MTVL2.8 Mini Project with Seminar

Elective-V

SYSTEM MODELLING & SIMULATION

Credits : 3

Subject Code :MTVL -3.1 III – Semester Course educational Objectives: The objectives of this course is

CEO 1: Define the basics of simulation modeling and replicating the practical situations in organizations

CEO 2:Develop simulation model using heuristic methods.

CEO 3: Generate random numbers and random variates using different techniques.

CEO 4: Analysis of Simulation models using input analyser, and output analyser

Course Outcomes: At the completion of the course the student will be able to

CO 1:Describe the role of important elements of discrete event simulation and modeling paradigm.

CO 2:Conceptualize real world situations related to systems development decisions, originating from source requirements and goals.

CO 3:Interpret the model and apply the results to resolve critical issues in a real world environment.

CO 4: Apply random number variates to develop simulation models

CO 5: Analyze output data produced by a model and test validity of the model

UNIT I

Basic Simulation Modeling :Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand basic simulation modeling

LO 2:explain discrete event simulation

UNIT II

SIMULATION SOFTWARE:

Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain simulation packages

LO 2: understand arena extend

UNIT III

BUILDING SIMULATION MODELS AND MODELING TIME DRIVEN SYSTEMS:

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility. Modeling input signals, delays, System Integration, Linear Systems,

Max. Marks :70 Sessionals :30 Motion Control models, numerical experimentation

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain motion control models

LO 2:understand model input signals

UNIT IV

EXOGENOUS SIGNALS AND EVENTS:

Disturbance signals, state machines, petri nets & analysis, System encapsulation, Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain disturbance signals

LO 2:understand time Markov processes

UNIT V

EVEN DRIVEN MODELS:

Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain simulation diagrams

LO 2: explain queuing theory

UNIT VI

SYSTEM OPTIMIZATION:

System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain system identification process

LO 2:understand simulation methodology

TEXT BOOKS:

- 1. System Modeling & Simulation, An introduction Frank L.Severance, John Wiley&Sons, 2001.
- 2. Simulation Modeling and Analysis Averill M.Law, W.David Kelton, TMH, 3rd Edition, 2003

REFERENCES:

Systems Simulation – Geoffery Gordon, PHI, 1978

Elective-V

EMI / EMC

Credits : 3

Subject Code :MTVL –3.1 III– Semester Max. Marks :70 Sessionals :30

Course educational Objectives: The objectives of this course is

CEO 1: To familiarize with the fundamentals that are essential for electronics industry in the field of EMI / EMC

CEO 2: To understand EMI sources and its measurements

CEO 3:To understand the various techniques for electromagnetic compatibility.

CEO 4:Acquire broad knowledge of various EM radiation measurement techniques.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Designing electronic systems that function without errors or problems related to electromagnetic compatibility.

CO 2:Diagnose and solve basic electromagnetic compatibility problems.

CO 3:Understand the effect of EM noise in system environment and its sources.

CO 4:Understanding about the functions of a ground, understanding about cables and connectors.

CO 5:Understanding the various aspects of shielding.

UNIT I

INTRODUCTION, NATURAL AND NUCLEAR SOURCES OF EMI / EMC:Electromagnetic Environment, History, Concepts, Practical Experiences and Concerns, Frequency Spectrum Conservations. An Overview of EMI / EMC, Natural and Nuclear Sources of EMI.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain electromagnetic environment

LO 2:understand practical experiences and concerns

UNIT II

EMI FROM APPARATUS, CIRCUITS AND OPEN AREA TEST SITES: Electromagnetic Emissions, Noise from Relays and Switches, Nonlinearities in

Circuits, Passive Intermodulation, Cross Talk in Transmission Lines, Transients in Power Supply Lines, Electromagnetic Interference (EMI). Open -Area Test Sites and Measurements.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain passive intermodulation

LO 2:explain EMI

UNIT III

RADIATED AND CONDUCTED INTERFERENCE MEASUREMENTS AND ESD: Anechoic Chamber, TEM Cell, Giga-Hertz TEM Cell, Characterization of Conduction Currents / Voltages, Conducted EM Noise on Power Lines, Conducted EMI from Equipment, Immunity to Conducted EMI Detectors and Measurements. ESD, Electrical Fast Transients / Bursts, Electrical Surges.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand radiated interference

LO 2:explain conducted interference

UNIT IV

GROUNDING, SHIELDING, BONDING AND EMI FILTERS: Principles and Types ofGrounding, Shielding and Bonding, Characterization of Filters, Power Line Filter Design. **Learning Outcomes:** At the end of the unit, the student will be able to

LO 1:understand grounding

LO 2:understand emi filters

UNIT V

CABLES, CONNECTORS, COMPONENTS AND EMC STANDARDS: EMISuppression Cables, EMC Connectors, EMC Gaskets, Isolation Transformers, Opto-Isolators, National/ International EMC Standards.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: understand cable connectors

LO 2: understand EMC connectors

TEXT BOOKS:

- 1. Engineering Electromagnetic Compatibility by Dr. V.P. Kodali, IEEE Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
- 2. Electromagnetic Interference and Compatibility IMPACT series, IIT– Delhi, Modules1–9.

REFERENCE :

1. Introduction to Electromagnetic Compatibility, Ny, John Wiley, 1992, by C.R. Pal.

Elective-V

HARDWARE-SOFTWARE CO-DESIGN

Credits: 4

Subject Code : MTVL – 3.1 III – Semester **Max. Marks :** 70 **Sessionals :** 30

Course educational Objectives: The objectives of this course is

CEO 1: Profound knowledge of the architectures of computer systems.

CEO 2: analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description,

Course Outcomes: At the completion of the course the student will be able to

CO 1: transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa,

CO 2: partition simple software programs into hardware and software components ,and create appropriate hardware-software interfaces to reflect this partitioning,

CO 3: identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components, and

CO 4: . use simulation software to co-simulate software programs with cycle-based hardware descriptions.

CO 5: explain the control-flow and data-flow of a software program and a cycle-based hardware description,

UNIT- I

CO-DESIGN ISSUES: Co-design Models, Architectures, Languages, A Generic Co-Design Methodology,

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1: explain codesign models
- **LO 2:** explain generic codesign methodology

UNIT- II

CO-SYNTHESIS ALGORITHMS: Hardware –Software Synthesis Algorithms: Hardware – Software Partitioning, Distributed System Co-Synthesis.

Learning Outcomes: At the end of the unit, the student will be able to

- **LO 1:** explain synthesis algorithms
- LO 2: explain cosynthesis

UNIT-III

PROTOTYPING, EMULATION AND TARGET ARCHITECTURES : Prototyping and emulation techniques, Prototyping and emulation environments future developments in emulation and prototyping, architecture specialization techniques, system communication infrastructure, Target Architectures And Application System Classes, Architectures For Control Dominated System And Data Dominated Systems.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: understand prototyping

LO 2: explain data dominated systems

UNIT –IV

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern Embedded Architectures, Embedded Software Development Needs, Compilation Technologies, Practical Consideration in a Compiler Development Environment

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: understand modern embedded architectures

LO 2: explain embedded software

UNIT- V

DESIGN SPECIFICATION AND VERIFICATION: The Co-Design Computational Model, Concurrency, Co-Coordinating Concurrent Computations, Interfacing Components, Design Verification, Implementation Verification, Verification Tools, Interface Verification.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1: explain co-design computational model
- LO 2: understand concurrency

UNIT- VI

LANGUAGES FOR SYSTEM-LEVEL SPECIFICATION AND DESIGN: System Level Specification, Design Representation For System Level Synthesis, System Level Specification Languages Heterogeneous Specifications And Multi Language Co-Simulation, The Cosyma System And Lycos System.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: understand system level specification

LO 2: explain system level design

TEXT BOOK:

1. Hardware/software co-design principles and practice, kluwer academic publishers

Open Elective

CELLULAR AND MOBILE COMMUNICATIONS

Credits: 3

Max. Marks :70 Sessionals :30

Subject Code :MTVL – 3.2 III– Semester

CourseeducationalObjectives: The objectives of this course is

CEO 1: To know the evolution of Mobile communication and cell concept to improve capacity of the system

CEO 2:To know the fading mechanism and types of fading and effect of fading on Mobile communication.

CEO 3:To know the role of equalization in Mobile communication and to study different types of Equalizers and Diversity techniques.

CEO 4:To know the types of channel coding techniques, data transmission modes and services of GSM.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:demonstrate knowledge on : cellular concepts like frequency reuse, fading, equalization, GSM ,CDMA

CO 2:demonstrate knowledge hand-off and infertace and apply the concept to calculate link budget using path loss model

CO 3:demonstrate knowledge equalization and different diversity techniques

CO 4: apply the concept of GSM in real time applications.

CO 5: compare different multiple access techniques in mobile communication

UNIT- I

Introduction to Wireless communications, examples of wireless communication system, the Cellular concept and system design fundamentals, Frequency reuse, channel assignment strategies, handoff strategies, Interference and system capacity, Trunk and grade services, Methods for improving coverage and capacity in cellular system.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand examples of wireless communications

LO 2: explain frequency reuse

UNIT-II

Multiple access techniques for wireless communications FDMA, TDMA, Spread spectrum techniques, SDMA, Packet Radio, CSMA, Capacity of cellular CDMA with multiple cells and capacity of SDMA.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain multiple access techniques

LO 2:explain CSMA

UNIT-III

Wireless systems and standards, AMPS, IS - 94, GSM traffic, Examples of GSM cell, Frame structure of GSM cell, Details of forward and reverse CDMA channels.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: explain AMPS

LO 2:explain GSM traffic

UNIT-IV

Personal access communication systems, personal Mobile satellite communications, Integrating Geo, LEO MEO satellite and terrestrial mobile systems, Rake receiver and Advanced Rake receiver,

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain PMSC LO 2:Explain LEO MEO satellite

UNIT-V

Mobile Radio Propagation, Large scale path loss, Reflection, Diffraction, Scattering, Outdoor and Indoor Propagation models, small signal fading and multi path, measurement of small scale path loss, parameters and multi path channels, fading due to multi path, fading effect due to Doppler spread, small scale fading models, equalization, Diversity.

Learning Outcomes: At the end of the unit, the student will be able to

- **LO 1:**explain large scale path loss
- LO 2:explain fading due to multipath

Text Book:

- 1. Mobile cellular communication by GottapuSasibhushan Rao, PERSON International, 2012.
- 2. Wireless communications Principles and Practice, Second Editions, THEODORE S.REPPAPORT.

REFERENCES:

- 1. Wireless Digital Communications, DR. KAMILO FEHER.
- 2. Electronic Communication system, WAYNE ToMASI.
- 3. Wireless Communications, SANJY SHARMS

OPEN ELECTIVE BUSINESS ANALYTICS

Subject Code : MTRM – 3.2

III– Semester Course educational Objectives: The objectives of this course is Credits : 3 Max. Marks :70 Sessionals :30

CEO 1: Investigate data to establish new relationships and patterns

CEO 2:Analyze the correlation between different variables **CEO 3:**Analyze the possibility of default and generate customer records **CEO 4:**Use tools such as Excel and open source to interpret data Course Outcomes: At the completion of the course the student will be able to

CO 1:Understand and critically apply the concepts and methods of business analytics

CO 2:Identify, model and solve decision problems in different settings

CO 3:Interpret results/solutions and identify appropriate courses of action for a given managerial situation whether a problem or an opportunity

CO 4:Create viable solutions to decision making problems

CO 5:nstil a sense of ethical decision-making and a commitment to the long-run welfare of both organisations and the communities they serve

Unit1: Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modelling, sampling and estimation methods overview.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain business analytics

LO 2:explain relationship of BA

Unit 2: Trendiness and Regression Analysis: Modelling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain regression analysis

LO 2:explain BA data models

Unit 3: Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modelling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modelling, nonlinear Optimization.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain organization structure

LO 2: explain outsourcing

Unit 4: Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis:

Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain forecasting techniques

LO 2:explain forecasting models

Unit 5: Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain decision analysis

LO 2:explain decision tress

Unit 6: Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain recent trends in

LO 2:understand visual data recovery

Reference:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.

2. Business Analytics by James Evans, persons Education

OPEN ELECTIVE INDUSTRIAL SAFETY

Subject Code : MTRM – 3.2

Credits : 3

Max. Marks :70 Sessionals :30

III– Semester Course educational Objectives: The objectives of this course is

 $CEO\ 1:$ To know about Industrial safety programs and toxicology, Industrial laws , regulations and source models

CEO 2:To understand about fire and explosion, preventive methods, relief and its sizing methods

CEO 3:To analyze industrial hazards and its risk assessment.

Course Outcomes: At the completion of the course the student will be able to

CO 1:Analyze the effect of release of toxic substances

CO 2:Understand the industrial laws, regulations and source models.

CO 3:Apply the methods of prevention of fire and explosions.

CO 4:Understand the relief and its sizing methods.

CO 5:Understand the methods of hazard identification and preventive measures.

Unit-I: Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Learning Outcomes: At the end of the unit, the student will be able to

- LO 1:explain industrial safety
- LO 2:explain safety control

Unit-II: Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Learning Outcomes: At the end of the unit, the student will be able to LO 1:explain replacement economy LO 2:explain service life of equipment

Unit-III: Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1: explain Wear and corrosion prevention

LO 2:explain side feed lubrication

Unit-IV: Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain fault tracing **LO 2:**explain fault finding activities

Unit-V: Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain periodic and preventive maintenance

LO 2: explain repairing schemes

Reference:

- 1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
- 2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
- 3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
- 4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

OPEN ELECTIVE OPERATIONS RESEARCH

Subject Code : MTRM – 3.2

Credits : 3

Max. Marks :70 Sessionals :30

III– Semester CourseeducationalObjectives: The objectives of this course is

CEO 1: Ability to understand and analyze managerial problems in industry so that they are able to use resources (capitals, materials, staffing, and machines) more effectively.

CEO 2:Knowledge of formulating mathematical models for quantitative analysis of managerial problems in industry.

CEO 3:Skills in the use of Operations Research approaches and computer tools in solving real problems in industry.

CEO 4:Mathematical models for analysis of real problems in Operations Research.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Be able to understand the application of OR and frame a LP Problem with solution – graphical and through solver add in excel (software)

CO 2:Be able to build and solve Transportation and Assignment problems using appropriate method.

CO 3:Be able to design and solve simple models of CPM and queuing to improve decision making and develop critical thinking and objective analysis of decision problems

CO 4:Be able to solve simple problems of replacement and implement practical cases of decision making under different business environments.

CO 5:Enables to take best course of action out of several alternative courses for the purpose of achieving objectives by applying game theory and sequencing model

Unit 1: Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Learning Outcomes: At the end of the unit, the student will be able to LO 1:explain optimization techniques LO 2:explain inventory control models

Unit 2: Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Learning Outcomes: At the end of the unit, the student will be able to LO 1:explain formulation of LPp LO 2:understand parametric programming

Unit 3: Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT

Learning Outcomes: At the end of the unit, the student will be able to LO 1: explain CPM/PERT LO 2:explain non linear programming model

Unit 4: Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Learning Outcomes: At the end of the unit, the student will be able to LO 1:explain scheduling

LO 2:explain geometric programming

Unit 5: Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation.

Learning Outcomes: At the end of the unit, the student will be able to LO 1:explain competitive models LO 2: explain graph theory

References:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008

2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.

3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008

4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009

5. Pannerselvam, Operations Research: Prentice Hall of India 2010 6. Harvey M Wagner,

Principles of Operations Research: Prentice Hall of India 2010

OPEN ELECTIVE Composite Materials

Subject Code : MTRM – 3.2

III– Semester CourseeducationalObjectives: The objectives of this course is

CEO 1: Explain the behavior of constituents in the composite materials

CEO 2:Enlighten the students in different types of reinforcement

CEO 3:Develop the student's skills in understanding the different manufacturing methods available for composite material.

CEO 4:Illuminate the knowledge and analysis skills in applying basic laws in mechanics to the composite materials.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Explain the mechanical behavior of layered composites compared to isotropic materials.

CO 2:Apply constitutive equations of composite materials and understand mechanical behavior at micro and macro levels.

CO 3:Determine stresses and strains relation in composites materials.

CO 4:Identify, describe and evaluate the properties of fiber reinforcements, polymer matrix materials and commercial composites.

CO 5:Analyze the elastic properties and simulate the mechanical performance of composite laminates; and understand and predict the failure behavior of fiber-reinforced composites

UNIT-I:

INTRODUCTION: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

Learning Outcomes: At the end of the unit, the student will be able to

Credits : 3 Max. Marks :70 Sessionals :30 **LO 1:**explain composite materials **LO 2:**explain functional requirements

UNIT – II:

REINFORCEMENTS: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

Learning Outcomes: At the end of the unit, the student will be able to

- **LO 1:** explain iso stress
- LO 2:understand reinforcement

UNIT – III:

Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain liquid phase sintering

LO 2: understand manufacturing of metal matrix components

UNIT-IV:

Manufacturing of Polymer Matrix Composites: Preparation of Molding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression molding – Reaction injection molding. Properties and applications.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain compression moulding

LO 2:explain polymer properties

UNIT – V:

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain strength

LO 2:explain stress concentrations.

TEXT BOOKS:

1. Material Science and Technology - Vol 13 - Composites by R.W.Cahn - VCH, West Germany.

2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

References:

- 1. Hand Book of Composite Materials-ed-Lubin.
- 2. Composite Materials K.K.Chawla.
- 3. Composite Materials Science and Applications Deborah D.L. Chung.
- 4. Composite Materials Design and Applications Danial Gay, Suong V. Hoa, and Stephen

W. Tasi.

OPEN ELECTIVE

Waste To Energy

Subject Code : MTRM – 3.2

III- Semester

Credits : 3 Max. Marks :70 Sessionals :30

CourseeducationalObjectives: The objectives of this course is

CEO 1: To enable students to understand of the concept of Waste to Energy
CEO 2:To link legal, technical and management principles for production of energy form waste.
CEO 3:To learn about the best available technologies for waste to energy.
CEO 4:To analyze of case studies for understanding success and failures.

CourseOutcomes: At the completion of the course the student will be able to

CO 1:Apply the knowledge about the operations of Waste to Energy Plants.
CO 2:Analyze the various aspects of Waste to Energy Management Systems
CO 3:Carry out Techno-economic feasibility for Waste to Energy Plants.
CO 4:Apply the knowledge in planning and operations of Waste to Energy plants.
CO 5:apply Centralized and Decentralized Waste to Energy Plant

Unit-I:

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:explain waste as fuel

LO 2:explain conversion devices

Unit-II:

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand biomass physics

LO 2:explain pyrolysis

Unit-III:

Biomass Gasification:Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand gasifier LO 2:explain biomass gasification

Unit-IV:

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand biomass combustion

LO 2:understand inclined grate combustors

Unit-V:

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Learning Outcomes: At the end of the unit, the student will be able to

LO 1:understand biogass

LO 2:explain properties of bio gas

References:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.

2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.

3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.

4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

Code	Name of the Subject	Periods/	Periods/Week		Max. Marks		Credits				
		Theory	Lab	Ext.	Int.						
MTVL3.3	Dissertation- I / Industrial Project	-	-	-	100	100	10				
IV-Semester											
Code	Name of the Subject Per	iods/Week	Μ	ax. Mar	ks	Total	Credits				

Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVL4.1	Dissertation-II	-	-	70	30	100	16